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Subject

Preventing Radiation-Induced MOSFET Failures Through Threshold Voltage Margin Analysis

Abstract

The Europa Clipper mission used specific power MOSFETs from Infineon that were specified for radiation total dose >100kRad. However, testing has shown that Infineon's "R5", "R6" and "R7" N-channel MOSFETs can fail at radiation levels lower than their specification under certain operating conditions. (Note that Infineon P-Channel MOSFETs were not affected, nor were older "R4" and newer "R9" Infineon N-channel MOSFETs).

Missions using MOSFETs in a radiation environment should include threshold-voltage-margin assessment in their design and review processes, regardless of the specific MOSFET supplier or radiation rating.

Threshold-voltage margin is often not explicitly analyzed in worst-case circuit analysis, even though a degraded threshold can directly cause failure.

Driving Event

In 2024, NASA was notified that some Infineon's N-channel MOSFETs, rated for 100 krad total ionizing dose (TID) were failing at radiation levels as low as 20 krad. NASA formed a cross-functional team (APL, JPL, and NESC) to analyze the Infineon MOSFET part-level radiation degradation and circuit-level failure susceptibility. There are several consequential effects from this finding, but most prominent is the nonlinear curve that relates the gate-to-source control voltage (Vgs) to MOSFET drain-source current conduction (Ids) is shifted such that it takes less Vgs voltage to achieve a given Ids current through the part. In the extreme case, the MOSFET can be on even with zero control voltage at its control terminal input, which precludes the MOSFET's ability to turn off.

Lessons Learned

The Infineon MOSFET issue caused a thorough review of the Europa Clipper design months before its successful launch on October 14th, 2024. In this review, all assemblies containing the affected MOSFETs were assigned risk levels that were determined by (1) radiation degradation testing of threshold voltage for each MOSFET part number and (2) circuit-level sensitivity to threshold voltage shift in each assembly.

Missions should first calculate threshold voltage margin, which is defined as the FET datasheet worst case (minimum) threshold voltage (Vgs_th) minus the application circuit's worst-case (highest) drive voltage while attempting to turn the FET off (Vol_max). The resulting voltage (Vth_margin) should be evaluated against the following criteria:

- For Infineon Generation R5 and R6 FETs, which typically have Vgs_th min = 2V
- For Infineon Generation R7 FETs, which typically have Vgs_th min = 1V

To illustrate the Europa Clipper review process, four examples of commonly used MOSFET gate drive circuits are discussed for circuit-level susceptibility to MOSFET threshold voltage shift.

1) Direct Drive MOSFET Gate

   The simplest type of MOSFET circuit is a low-side N-Channel MOSFET (source connected to circuit ground) with

its gate directly driven on/off from a gate drive circuit. These are the easiest circuits to analyze, as the first-order calculation of MOSFET threshold voltage margin is simply the minimum specified Vth minus the highest possible driver output voltage while driving low (Vol_max).

MOSFET gate drivers can originate from a variety of circuits and component types like: FPGAs, logic gates, and dedicated gate drive integrated circuits. Note that gate driver datasheets provide the Vol_max at a specified sink current, which is typically much greater than the gate drive circuits. This makes the analysis conservative. For a more realistic analysis, the gate driver IBIS models can be used to calculate the driver Vol_max at the gate driver's operating sink current in the specific application. A representative circuit is shown in Figure 1.

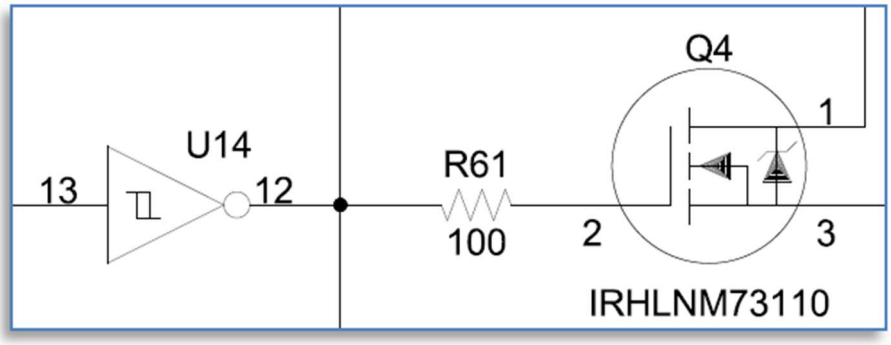


Figure 1. Example of Directly Driven Low-Side FET Circuit

In Figure 1, the N-FET gate is driven by a UT54ACTS14E Inverter (0 to +5V nominal), which is specified to have a worst-case low-driving output voltage (Vol_max) of 0.25V. Therefore, in the worst case, the N-FET (IRHLNM73110, Generation R7) gate voltage is 250 mV. The circuit will not be able to turn the N-FET off if the N-FET threshold voltage (Vth) drops from its minimum specification of 1V min to 250 mV, a radiation-induced degradation of 0.75V.

2) MOSFET Linear Regulator Circuits

The affected N-Channel MOSFETs can be used as linear regulators. In these circuits, an external control element such as an operation amplifier (op amp) is used to control the MOSFET's gate to-source voltage. Linear regulator circuits typically operate the MOSFET Vgs at voltages close to the threshold voltage, where the MOSFET conductivity is most sensitive to Vgs changes.

The effect of radiation-induced Vgs_threshold changes is mitigated in these linear regulator circuits because the control circuit uses negative feedback to set the operating point of the circuit. Therefore, if the MOSFET Vgs_threshold decreases, the control circuit will decrease the applied Vgs to maintain a regulated output. However, the op amp adjustability is limited by the op amp supply voltage, the minimum op amp output voltage, and the external circuit elements.

The linear regulator MOSFET circuits will fail when the threshold voltage degrades such that the op amp will not be able to turn the FET off with zero gate voltage. However, since the N-FET linear regulator uses its source terminal as its output voltage, the quiescent gate-to-source MOSFET voltage is the linear regulator output voltage plus the MOSFET threshold voltage. Therefore, linear regulators were among the most resilient circuits to radiation degradation because the non-zero source terminal voltage adds margin to the threshold voltage calculation.

3) Gate Drive Transformer Circuit Voltage Drop

The affected MOSFETs can be used in circuits with gate drive transformers. Gate drive transformers present several unique challenges for circuit analysis, including transient behavior and magnetic component modelling. In these circuits, a MOSFET is used to drive pulses across the primary of the gate drive transformer. The gate drive transformer secondary is connected to another MOSFET gate. In a typical circuit arrangement, series capacitors block dc signals from saturating the gate drive transformer and clamping diodes restore the dc on

the secondary side. These components and their variations must be studied.

During the circuit review, the Europa Clipper team identified circuits where an ac-coupled gate drive transformer circuit had unacceptably high output voltage. Specifically, the gate drive circuit waveform exhibited a “rebound” voltage in the off state due to voltage drops in the ac coupling circuit. An example gate drive transformer circuit is shown in Figure 2.

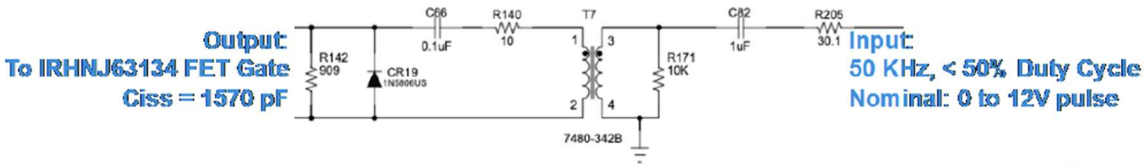


Figure 2. Example Gate Drive Transformer Circuit

The Figure 2 circuit uses a gate-drive transformer to drive a IRHNJ63134 Generation R6 N-FET gate from a PWM controller. The PWM controller drives 0 to +12V pulses at 50 KHz, with variable duty cycle up to 50% maximum. The gate drive transformer input is AC coupled (1uF coupling capacitor and a 30.1 Ohm resistor) to prevent transformer saturation.

If the PWM controller outputs 0 to +12V pulses at 50% duty cycle, the average (dc) voltage is 6V. The 1uF coupling capacitor charges to -6V to ensure that there is no dc component across the gate drive primary. The gate drive secondary has the same waveform shape with no dc component (-6 to +6V). However, this waveform could not be applied directly to the MOSFET gate, because the gate drive voltage too low. Therefore, the gate drive transformer has the unfortunate side effect that the peak output voltage is a function of the duty cycle.

To eliminate this undesirable behavior, a capacitor and diode are used on the gate drive transformer secondary to clamp the gate drive transformer output to “restore” the dc voltage in the original circuit. The secondary dc restorer charges the secondary-side capacitor to -6V to apply the +0 to +12V waveform to the MOSFET gate. Figure 3 shows the example gate drive circuit LTSpice model.

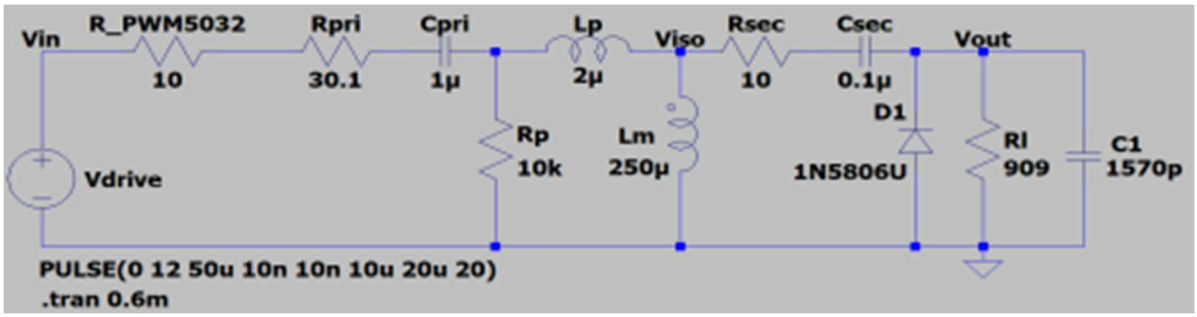


Figure 3. Example Gate Drive Transformer Circuit LTSpice Model

In Figure 3, the output resistance of the PWM controller is modelled as a 10 Ohm resistor. The IRHNJ63134 MOSFET is modelled as its datasheet input capacitance (1570pF). The gate drive transformer is modelled as a parallel magnetizing inductance (250 uH) calculated using its toroidal core dimensions, the number of primary/secondary turns, and core material magnetic permeability. The series leakage inductance (2 uH) is estimated as a percentage (0.8%) of the magnetizing inductance. The LTSpice simulation results are shown in Figure 4.

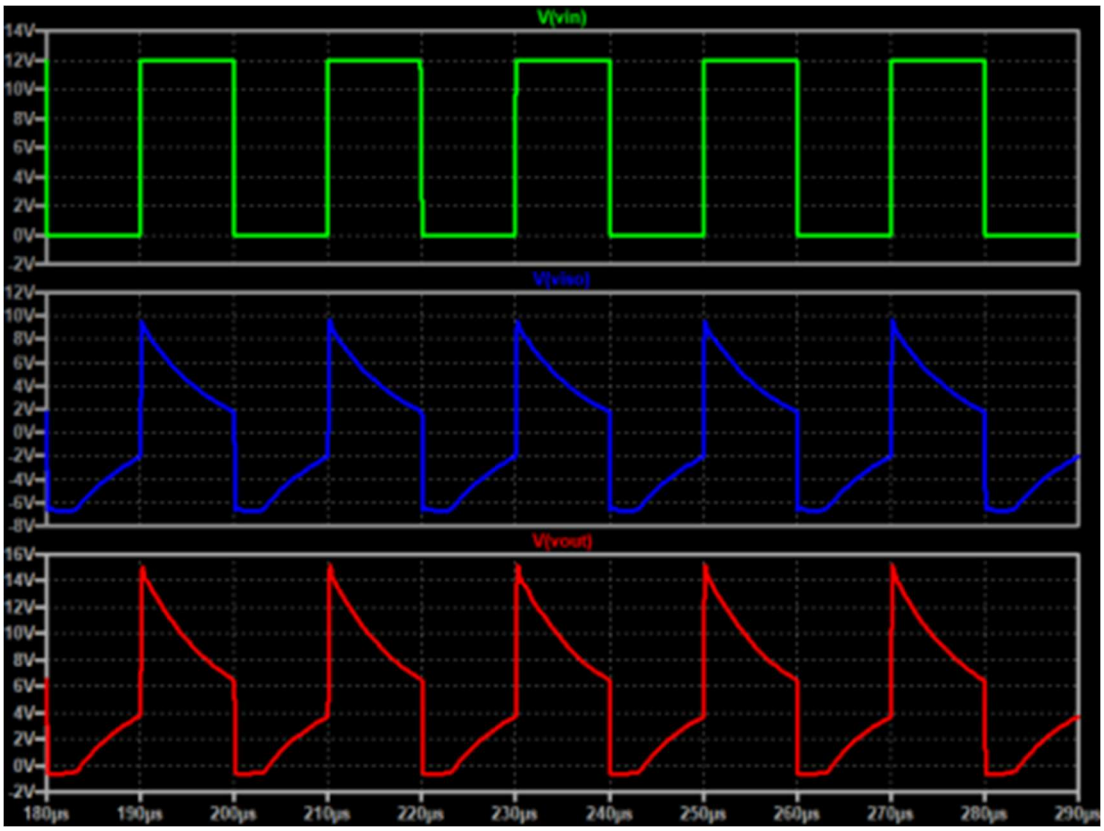


Figure 4. Gate Drive Circuit LTSpice Simulation (Green – Gate Drive Input from PWM Controller. Blue – Gate Drive Transformer Output Voltage. Red – MOSFET Gate-Source Voltage)

Figure 4 shows that the example circuit has unacceptably high output voltage in the off state (~4V) that exceeds the Vgs_threshold voltage and turns on the FET. Specifically, the gate drive circuit waveform exhibits an upward-sloping voltage in the off state due to voltage drop in the gate drive transformer circuit. The circuit also has a downward-sloping voltage in the on state that has unacceptably low voltage to keep the MOSFET on.

The root cause of the gate drive transformer circuit's distortion (downward slope during the "on" time, upward slope during the "off" time) is voltage drop in the equivalent circuit. The magnetizing inductance has a finite inductance, which necessarily draws current to accomplish transformer action. This current, however, creates voltage drop across the primary resistance and primary capacitance that results in the observed waveform distortion.

There are two competing concerns with this circuit. First, the circuit ringing is minimized when $R_{pri} \geq 2\sqrt{\frac{L_m}{C_{pri}}}$.

For the circuit values modelled, the critical damping value is Rpri = 32 Ohms. However, this resistance value may create excessive voltage drop. There is a tradeoff between reducing Rpri to lower distortion in the output voltage and maintaining Rpri high enough to avoid ringing that could cause MOSFET gate voltage stress. (Alternatively, note that the primary capacitance value can be increased to reduce the circuit impedance.)

Using the LTSpice model, the example circuit was modified to reduce the impedance of the gate drive circuit by changing Rpri from 30.1 Ohms to 4.99 Ohms. This reduced the voltage drop in the gate driver output circuit, at the expense of increasing the worst-case output ringing from 16V peak to 18V peak. Figure 5 shows the modified gate driver transformer circuit, and a simulated comparison between the original and modified gate drive output.

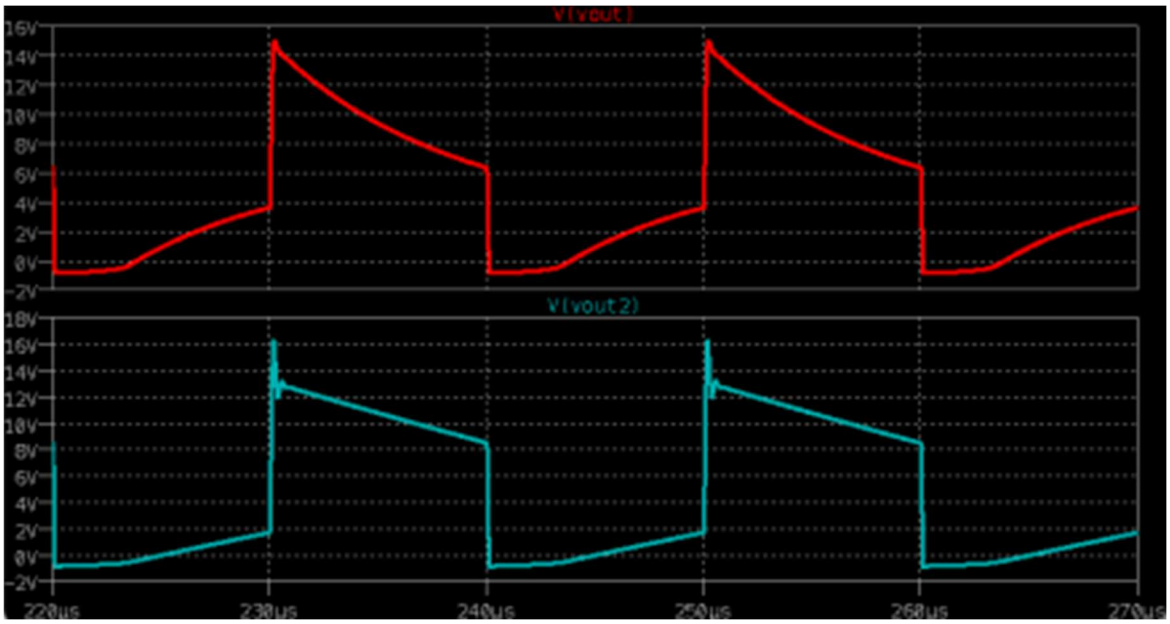


Figure 5. Modified Gate Drive Circuit LTSpice Simulation Results
(Red – Original Circuit Gate Drive Output. Cyan – Modified Circuit Gate Drive Output

Figure 5 shows that the modified circuit has approximately 2V higher minimum voltage in the "on" state and approximately 2V lower maximum voltage in the "off" state. This is at the expense of higher maximum ring voltage in the on state because the modified circuit is underdamped. Therefore, the circuit modification and tradeoffs met the redesign goals. Note that MOSFET Vgs_threshold degradation may require that the off-state voltage is held below the Vgs_threshold datasheet value.

4) Gate Drive Transformer Circuits with DC Restorer Circuits

Extreme caution should be used for ac-coupled gate drive transformer circuits with "dc restorer" circuits on the gate driver output. These gate drive transformer circuits are susceptible to overshoot during abrupt duty cycle changes that occur during startup and shutdown, which can cause inadvertent FET turn on. In an abrupt shutdown, like an overload on the converter output, the PWM controller duty cycle collapses from 50% to 0%. However, the capacitors in the gate drive circuit cannot change their voltage instantaneously. This causes a "rebound" transient in the N-FET gate-source voltage that may cause the N-FET to inadvertently turn on. Figure 6 shows this using the LTSpice model.

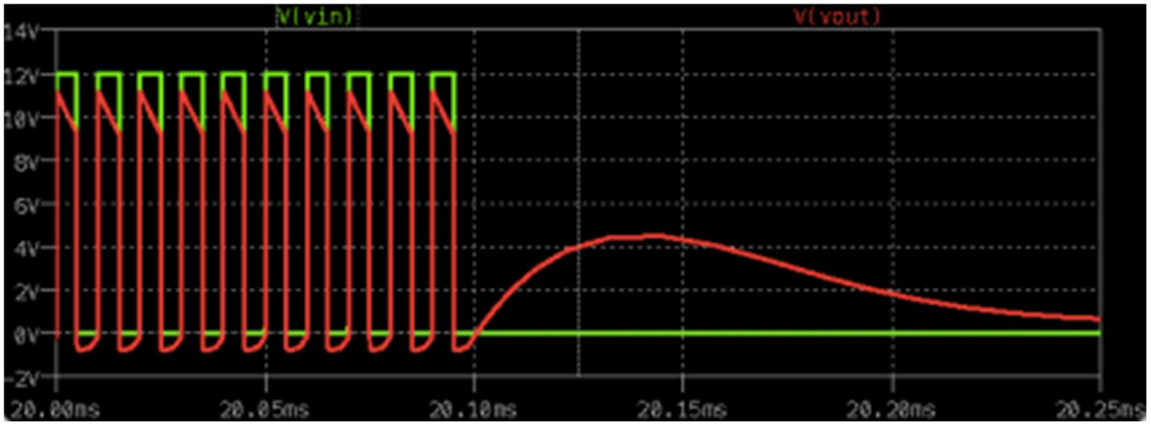


Figure 6. Gate Drive Circuit LTSpice Simulation During Abrupt Turn-Off
(Green – Gate Drive Input from PWM Controller. Red – MOSFET Gate-Source Voltage)

Figure 6 shows that abrupt turn-off causes the FET Vgs to exceed 2V for approximately 100 us. This inadvertent FET turn on can cause high currents in the FET in flyback and forward converters. In half bridge, full bridge, and

synchronous converters, this can turn on high-side and low-side FETs simultaneously, creating a shoot-through fault. Therefore, “dc restorer” circuits on gate drive transformers should be avoided. If this circuit must be used, conduct analysis of worst-case duty cycle transients to ensure that there is no device overstress or shoot through in the application. Note that MOSFET Vgs_threshold degradation may create larger transient currents for longer durations for a given rebound transient.

Recommendations

The following recommendations were developed from the Europa Clipper experience:

1) The Vgs threshold datasheet parameter is not always analyzed as a margined parameter in worst case circuit analysis (WCCA). This contrasts with parameters like maximum breakdown voltage, which is always included in worst case analysis and derating analysis. Therefore, circuit designers are typically unaware of the Vgs threshold margin of circuits. Missions should analyze their circuits for Vgs threshold margin.

2) Different gate drive circuit topologies (direct drive, gate drive transformer, etc) have sensitivities to Vgs threshold voltage that must be quantified by analysis and/or test.

3) Some applications use MOSFET in a bridge configuration (high-side and low-side) FETs that have a failure mode in which high-side and low-side MOSFETs are on at the same time, typically called “shoot-through”. The risk of shoot through should be quantified by analysis and/or test.

4) Missions should use analysis and/or test to demonstrate robustness of gate drive transformer circuits. Gate drive transformers have voltage drop that reduce threshold voltage margin, and gate drive “restorer” circuits can create a false turn-on signal during rapid duty cycle changes like startup and shutdown.

Topic(s)

- Engineering Design
- Integration and Testing
- Missions and Systems Requirements Definition
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- Systems Engineering and Analysis
- Flight Equipment
- Hardware
- Payloads
- Risk Management / Assessment
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