MEMS Deformable Mirror Development

Iris AO, Inc.

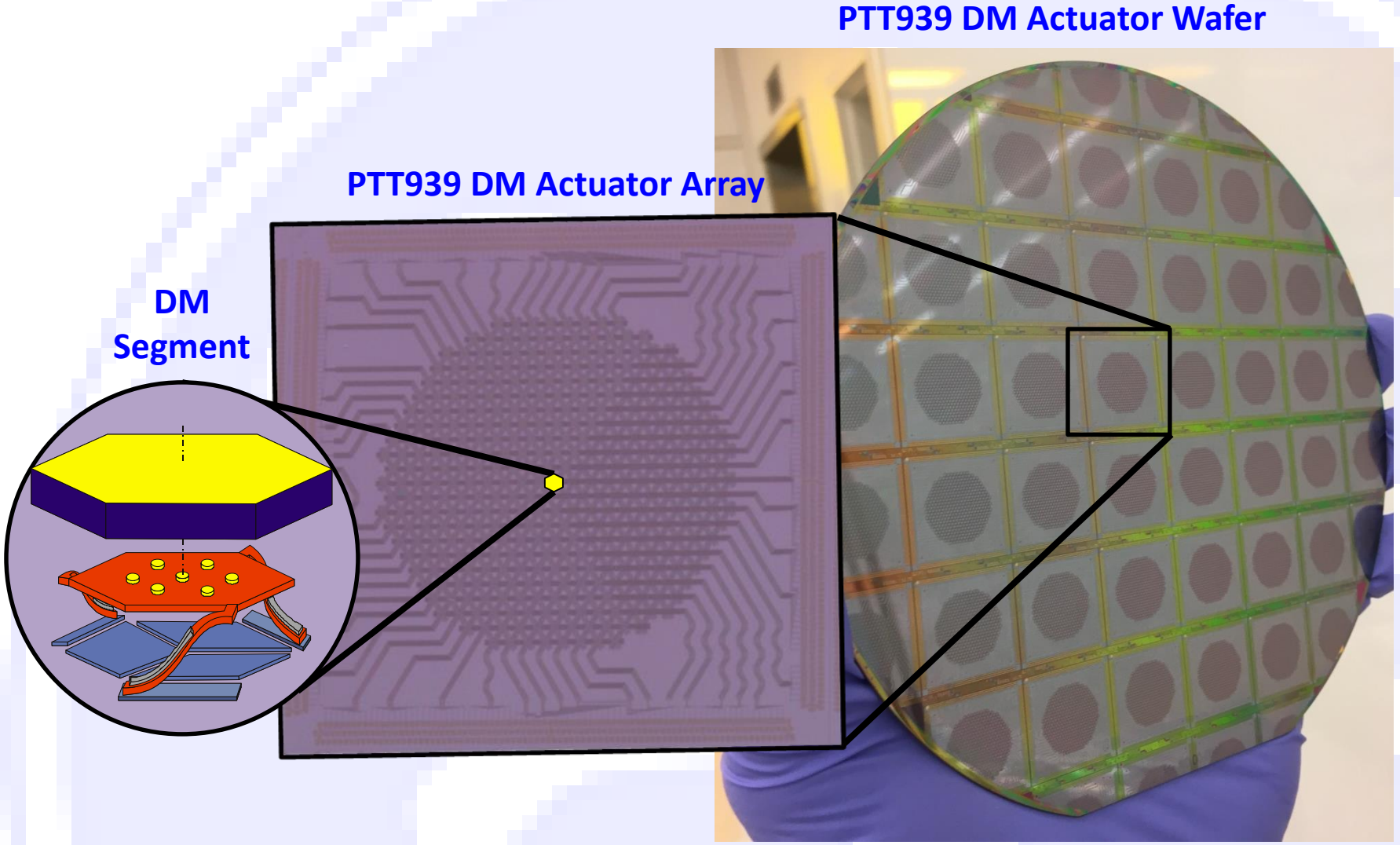
NASA Phase SBIRs: NNX14CG06C, NNX16CD58P
SAT/TDEM

Michael A. Helmbrecht
Iris AO, Inc.

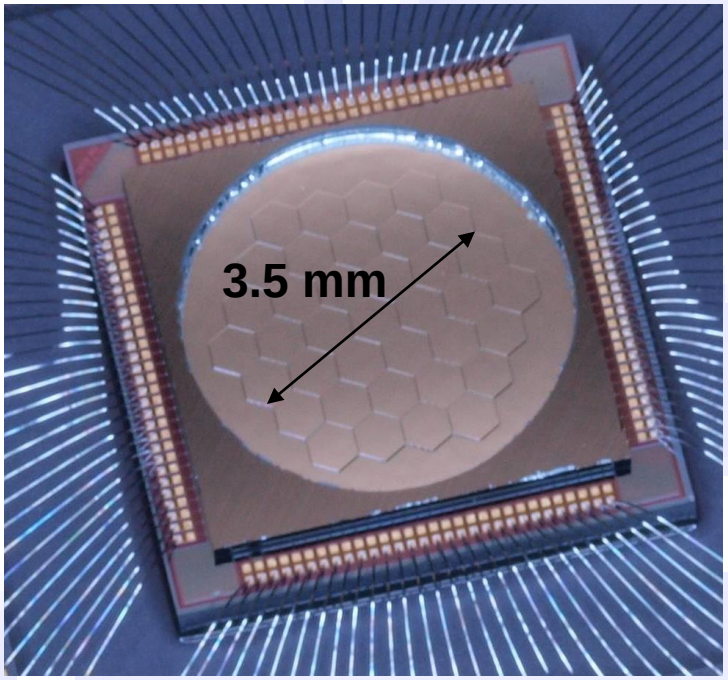
www.irisao.com
michael.helmbrecht@irisao.com
info@irisao.com

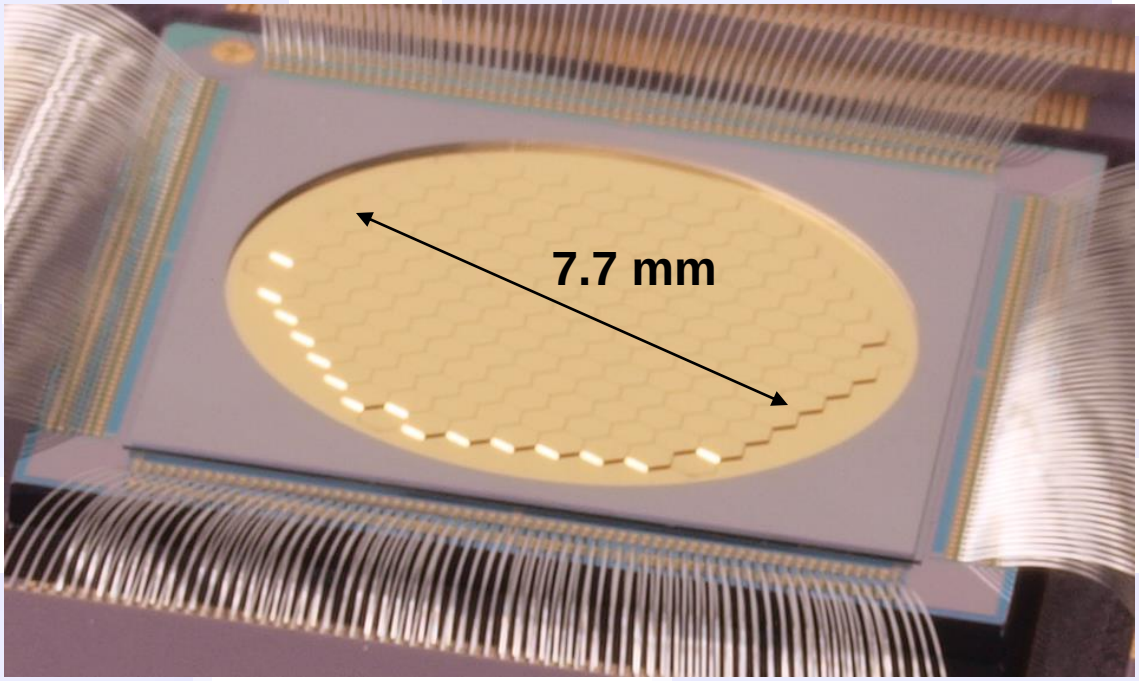
Iris AO Segmented DM Background

Silicon Wafer Processing



Iris AO MEMS Segmented Deformable Mirrors



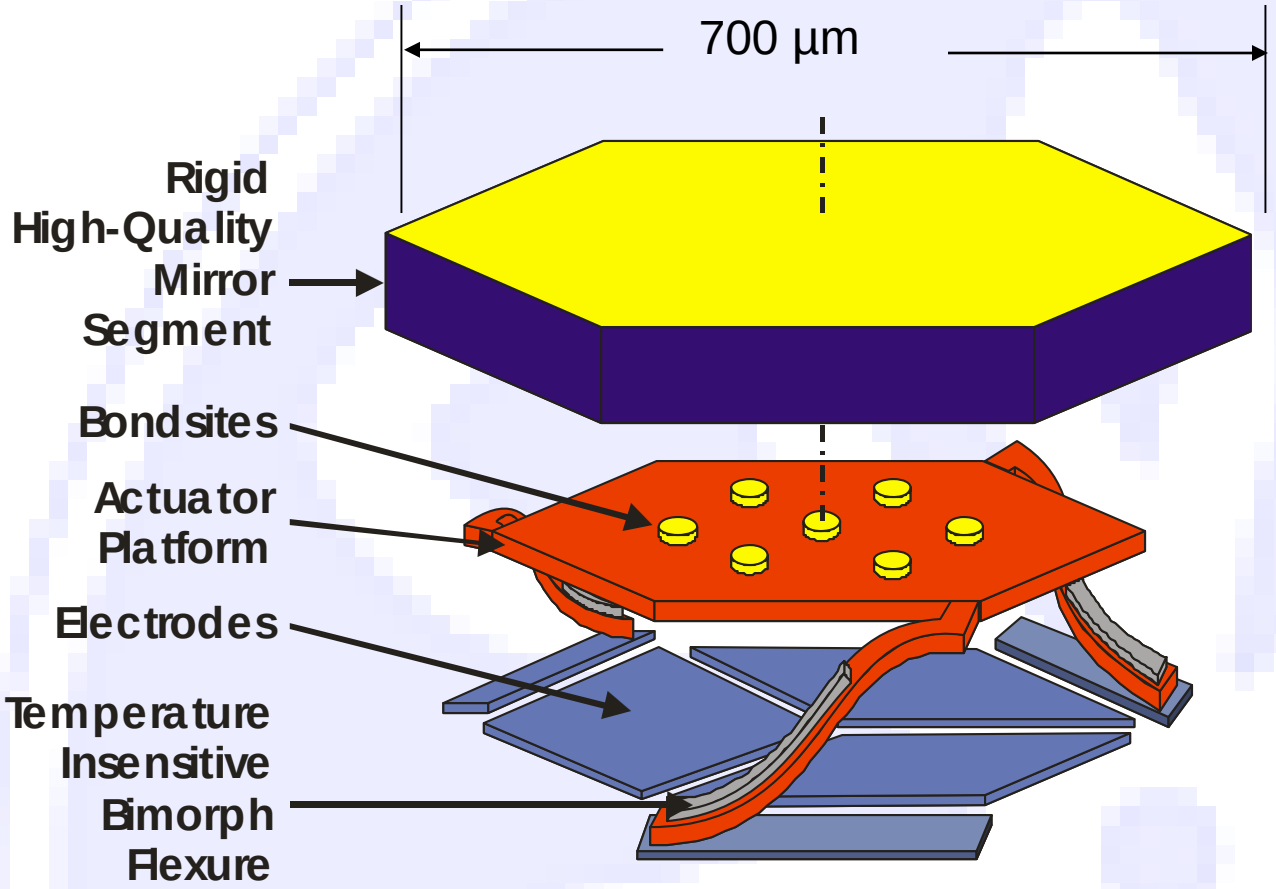


PTT111 DM
- 111 Actuators
- 37 PTT Segments
- 3.5 mm inscribed aperture
- Factory calibrated

PTT111L DM (Not Shown)
- 111 Large Format Actuators
- 37 PTT Segments
- 7.0 mm inscribed aperture
- Factory calibrated

PTT489 DM
- 489 Actuators
- 163 PTT Segments
- 7.7 mm inscribed aperture
- Factory calibrated

Iris AO Segmented DM Background



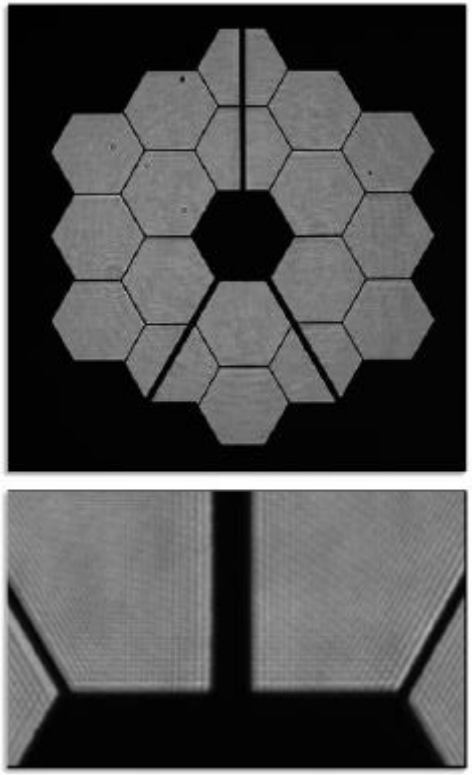
- 3 DOF: Piston/tip/tilt electrostatic actuation
  - no hysteresis
- Hybrid fabrication process
  - 3-layer polysilicon surface micromachining
  - Single-crystal-silicon assembled mirror
- Unit cell easily tiled to create large arrays
- Hybrid technology
  - Thick mirror segments
  - <1 nm PV/°C segment bow
  - Enables back-side stress-compensation coatings

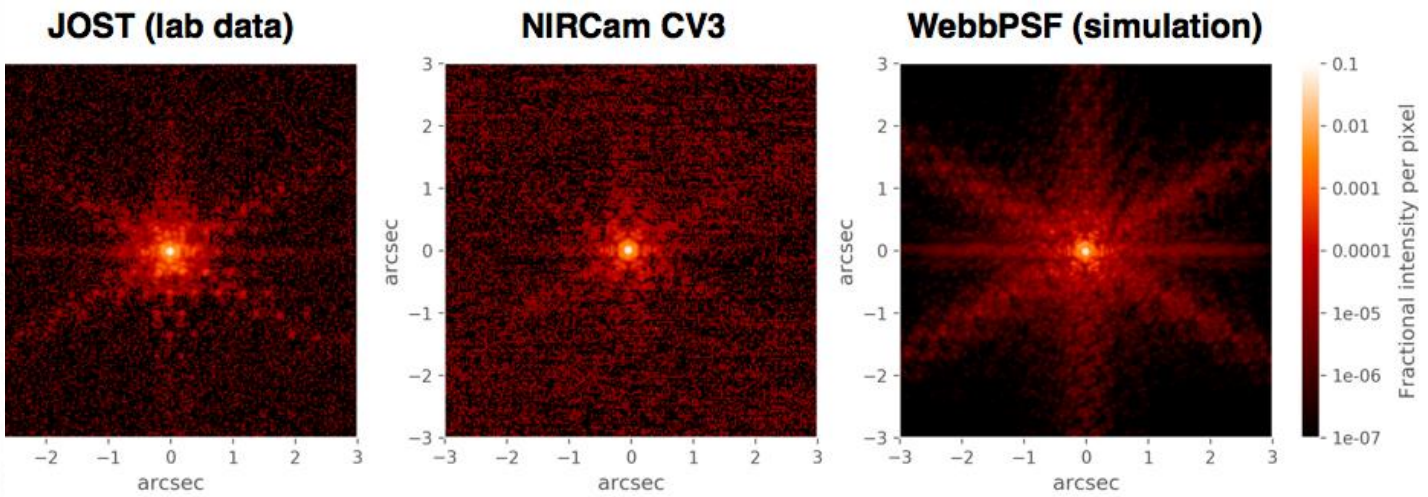
DM calibration holds >30 months, http://arxiv.org/abs/1609.04742
Recent Update: > 48 months and calibrations hold!

PTT111L Used for JWST Simulation

James Webb Space Telescope optical simulation testbed IV: linear control alignment of the primary segmented mirror

Sylvain Egron[a,b,c], Rémi Soummer[a], Charles-Philippe Lajoie[a], Aurélie Bonnefois[b], Joseph Long[a], Vincent Michau[b], Elodie Choquet[d,e], Marc Ferrari[c], Lucie Leboulleux[a,b,c], Olivier Levecq[a], Johan Mazoyer[a], Mamadou N'Diaye[f], Marshal Perrin[a], Peter Petrone[a], Laurent Pueyo[a], and Anand Sivaramakrishnan[a]

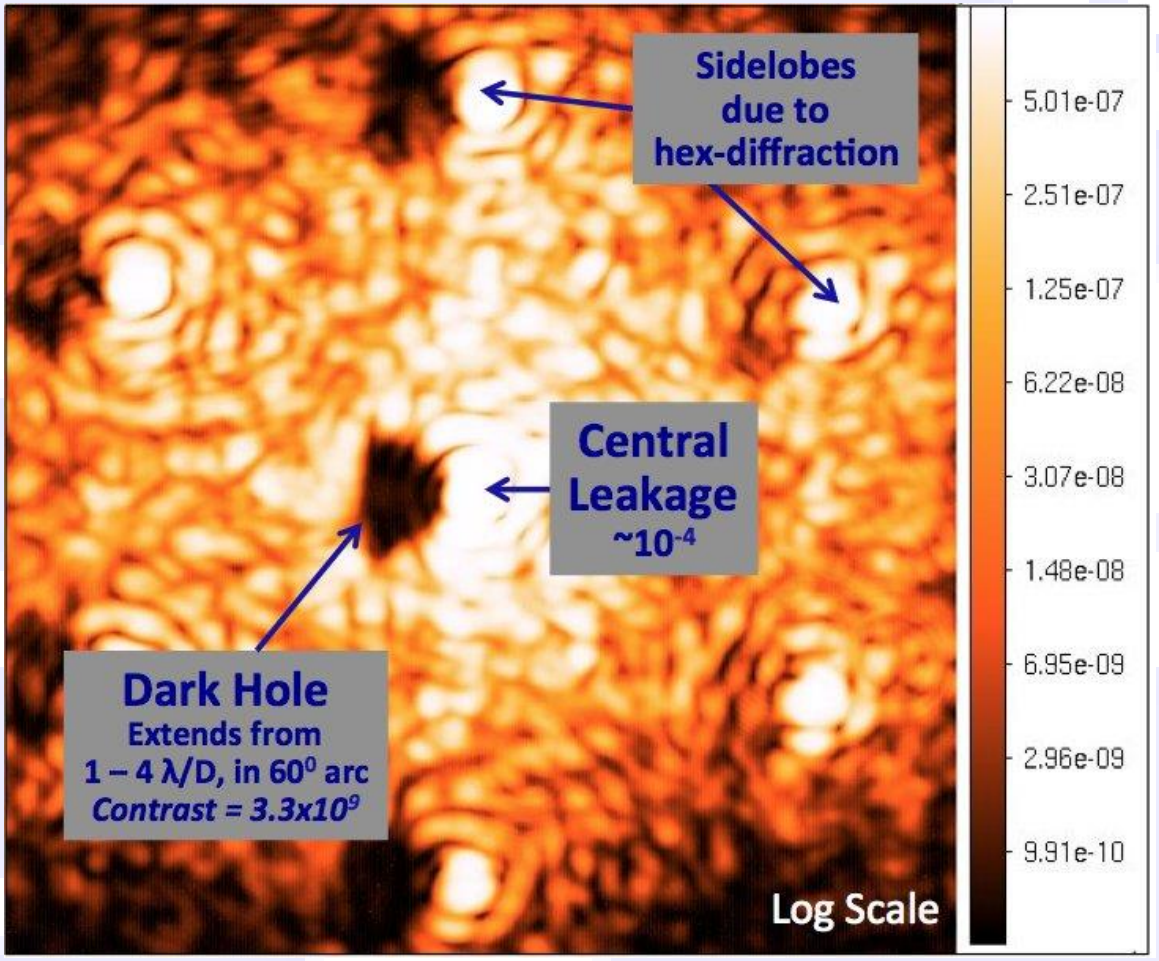




PTT489 Used for Visible Nulling Coronagraph

R.G. Lyon, M. Clampin, P. Petrone, U. Mallik, T. Madison, M.R. Bolcar, "High Contrast Vacuum Nuller Testbed (VNT) Contrast, Performance and Null Control," Proc. of SPIE 8442 (2012).

Highest contrast ever demonstrated with a MEMS DM!



10^9 Contrast @ IWA 1 – 4 λ/D Results
GSFC VNC Instrument on 06/09/12

SAT/TDEM Environmental Testing

TDEM Progress

- Prior Results
  - Developed FEM models of the MEMS actuators and mirror segments
    - Models match platform heights to within 6% and capture manufacturing non-idealities
  - In-house vibration, shock, and acoustic testing
    - DMs pass levels required by TDEM program
  - Issues with fabricating test devices: large process variations due to process immaturity
    - Issues from multiple lots identified and processes improved
- Current Effort
  - Manufacturing samples for testing
    - Materials appear to be the best to date
- Remaining Effort
  - Complete characterization at Iris AO and GSFC
  - Environmental testing
  - Post-test characterization
  - Final report

Additional Environmental Testing

- PTT489 DMs passed radiation testing
- PTT111 DM operation tested at -50°C
- PTT111 DM operation tested at 160 K and high vacuum (10^{-5} Torr)
  - http://www.mdpi.com/2072-666X/8/8/233
  - http://arxiv.org/abs/1704.03836
- PTT111-5 will be incorporated into a coronagraph on the High-Contrast Imaging Balloon System (HiCIBaS)
  - U Laval, U Leiden, U Montreal, U Victoria, CSA, ABB, Iris AO, JPL, Nüvü
  - Operation at 30-42 km elevation
  - Launch date: September 2018

Phase II SBIR Development NNX14CG06C

Increasing Phase Resolution

High-Resolution Electronics Development

- Existing Iris AO drive electronics are 14-bit resolution with integrated DAC / HV Amp

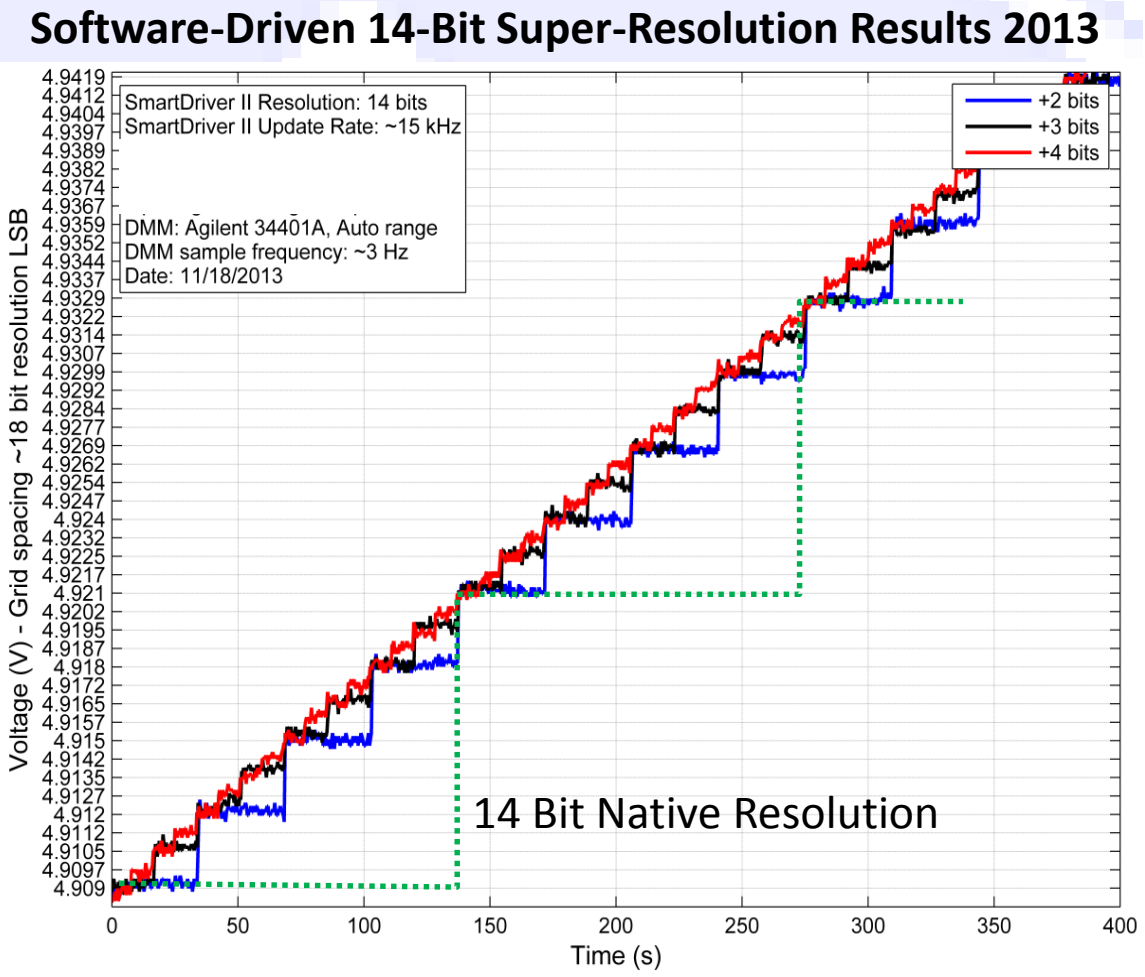
NNX14CG06C Development

- 16-bit resolution HV driver card
  - ADI 16-bit DAC + SuperTex HV Amp

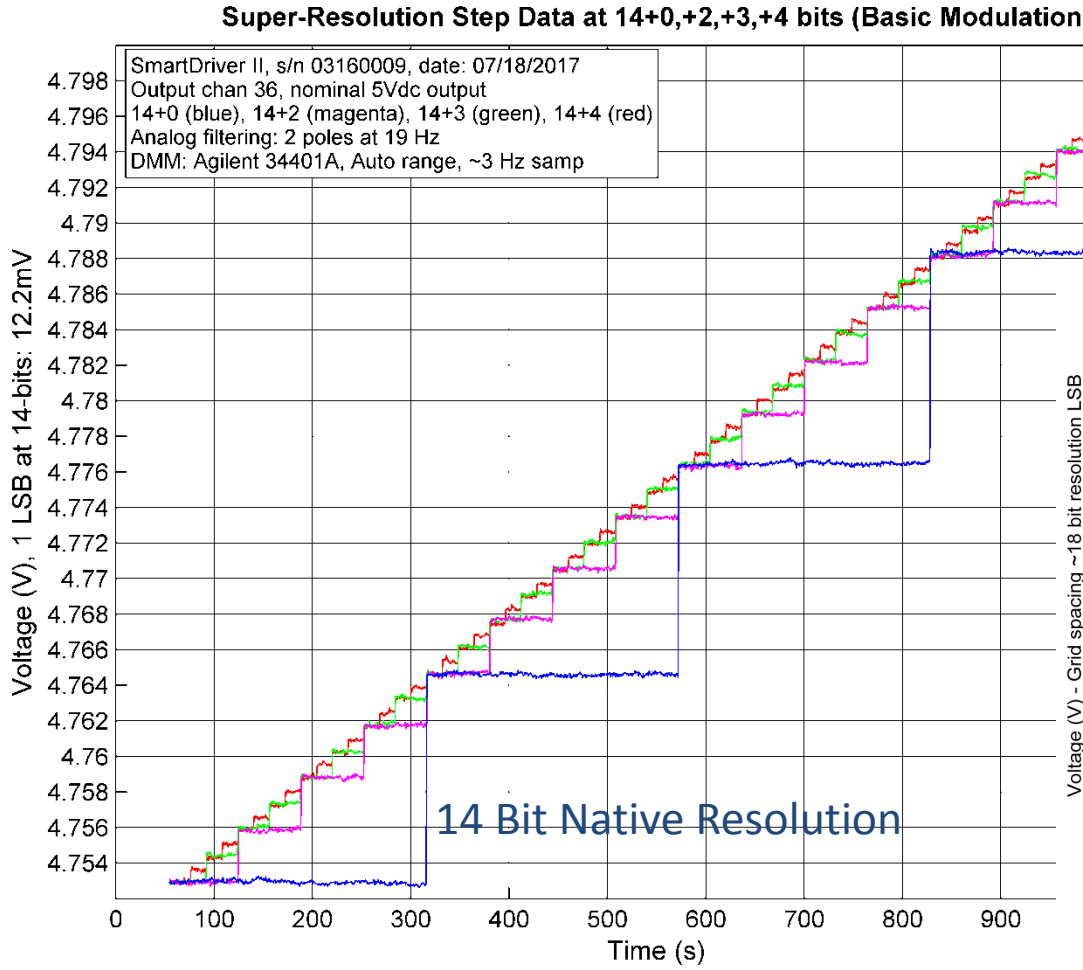
- USB2.0 High-Speed interface
  - Microcontroller
  - FPGA to implement timing critical modulation
  - Windows ***and*** Linux compatible
    - ~4 kHz updates under Linux

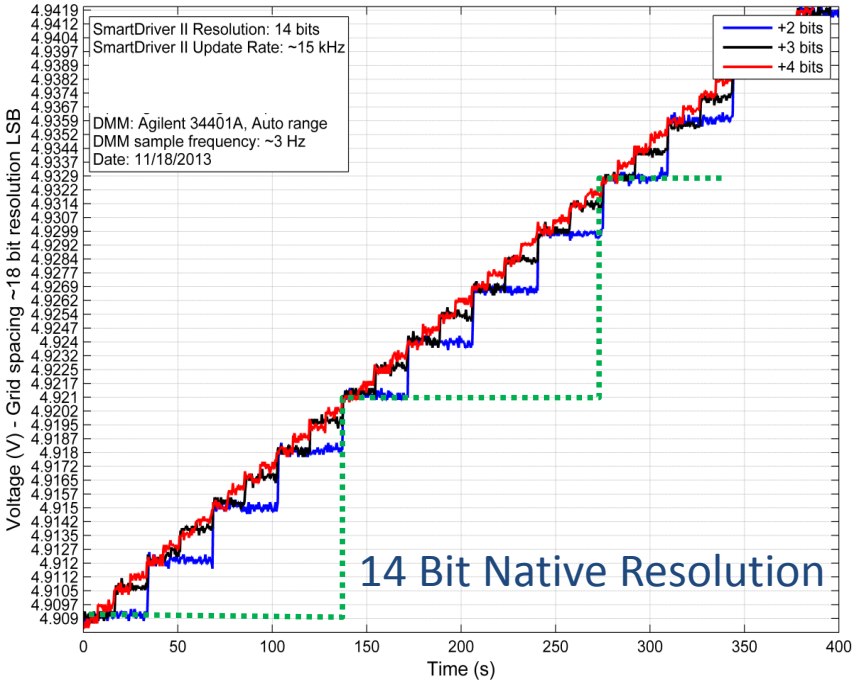
Super-Resolution Drive Electronics

- Iris AO electronics are 14 bit (native) resolution
- Super-resolution technique has demonstrated 18-bit resolution
  - Grid spacing is for 1 LSB on 18-bit resolution
  - Software driven control using a PCI interface card
  - Impractical for actual use
- Phase II Development
  - Modulation schemes implemented in FPGA on USB interface card



2017 Firmware vs 2013 Software



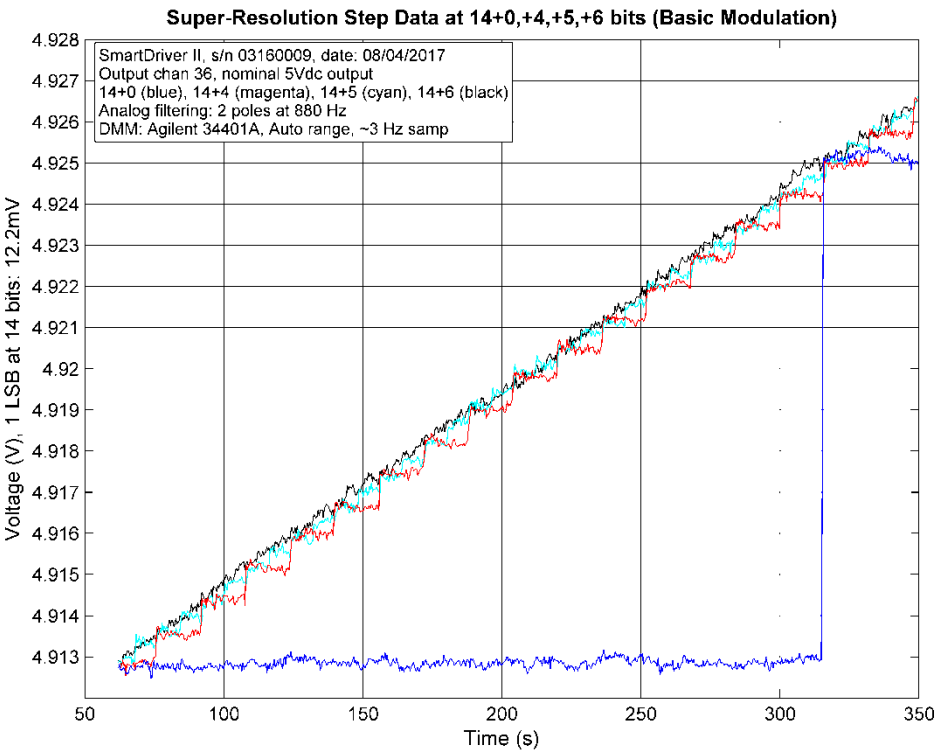


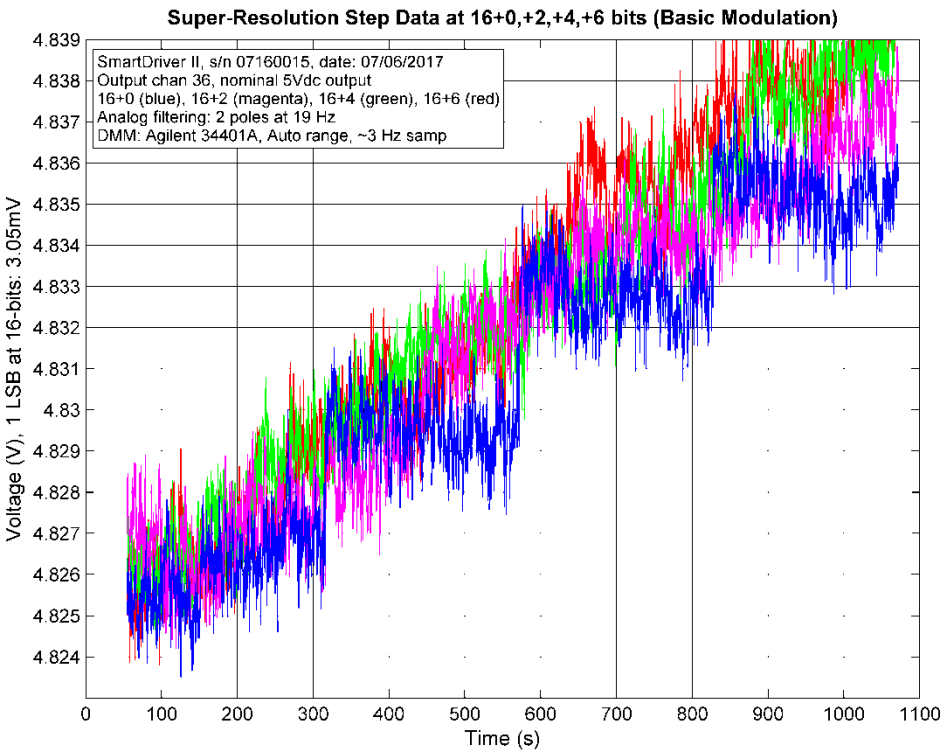
Firmware Control 2017

Software Control 2013

Firmware controlled super-resolution is better than PCIe computer interface hardware using software/DMA writes

Super Resolution: 14 vs 16 Bit Electronics



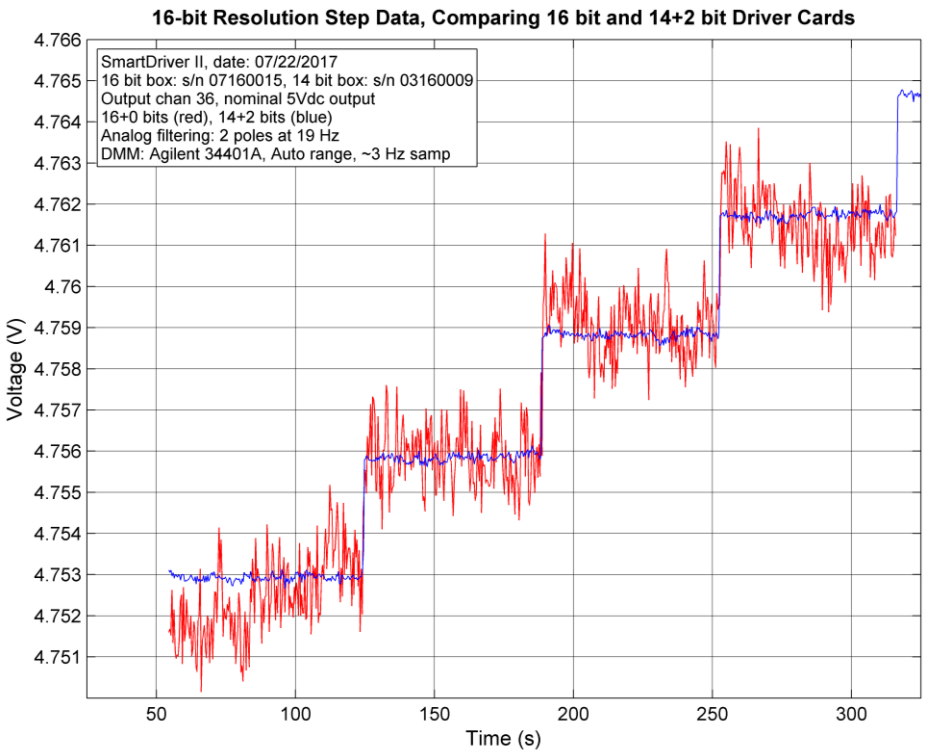


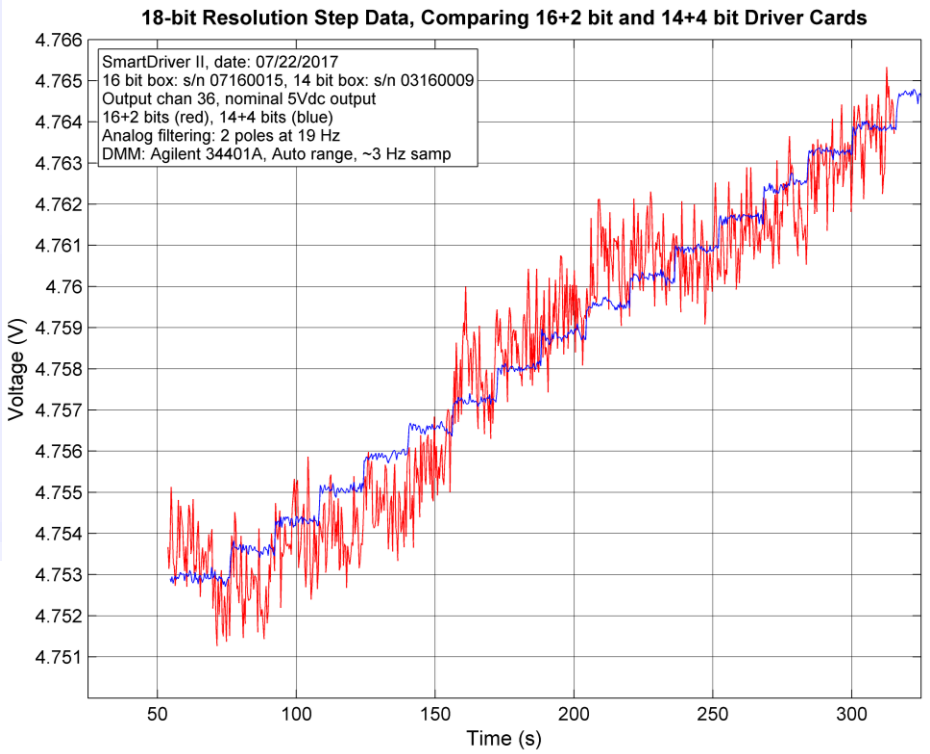
Iris AO Integrated 14 bit Electronics

ADI + SuperTex 16 bit Electronics

Iris AO 14-bit electronics with integrated DAC/HV Amp greatly outperform the ADI DAC + SuperTex HV Amp two-chip solution!

Super Resolution: 14 vs 16 Bit Electronics



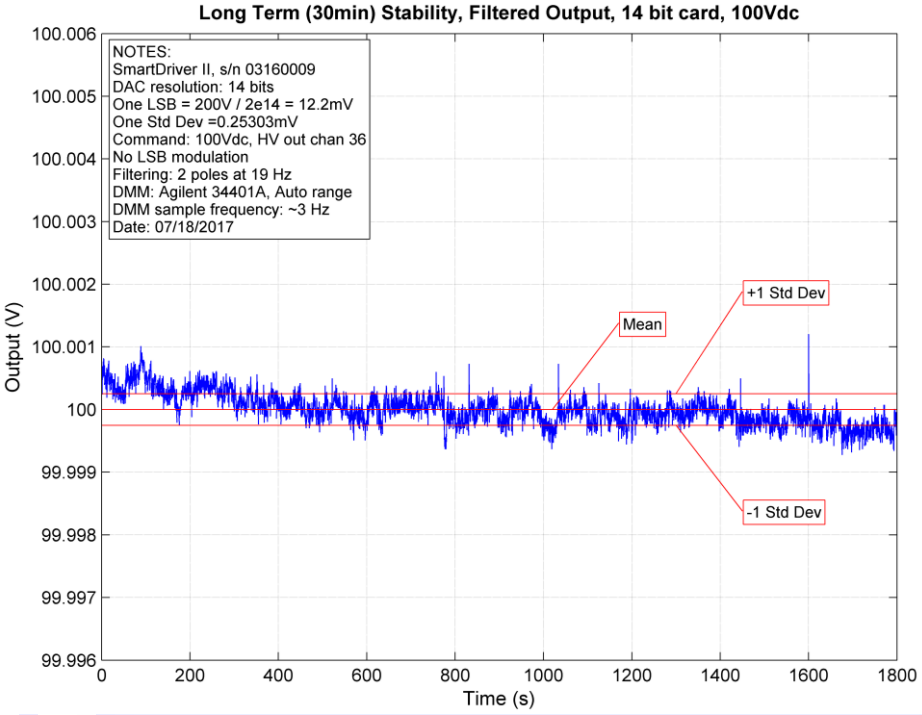


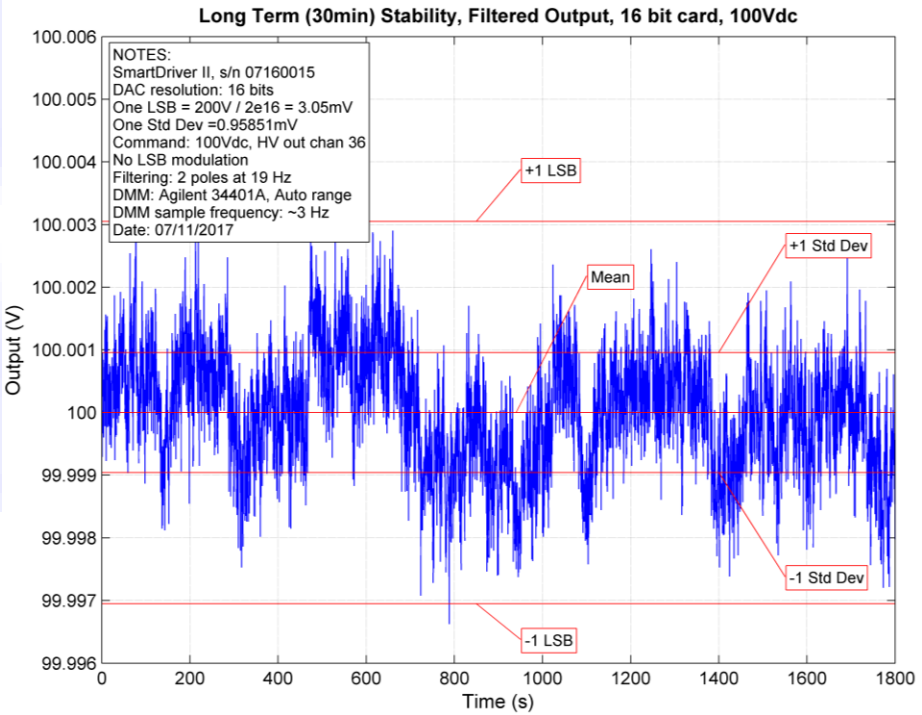
14 bit + 2 (blue) vs 16 bit (red)

14 bit + 4 (blue) vs 16 bit + 2 (red)

Iris AO 14-bit electronics with integrated DAC/HV Amp greatly outperform the ADI DAC + SuperTex HV Amp two-chip solution!

14 bit vs 16 bit Stability (30 min)





Iris AO Integrated 14 bit Electronics

- **std dev = 0.253 mV**
- **200 V max output**
- **19.6 bit stability over 30 minutes**

ADI + SuperTex 16 bit Electronics

- **std dev = 0.959 mV**
- **200 V max output**
- **17.7 bit stability over 30 minutes**

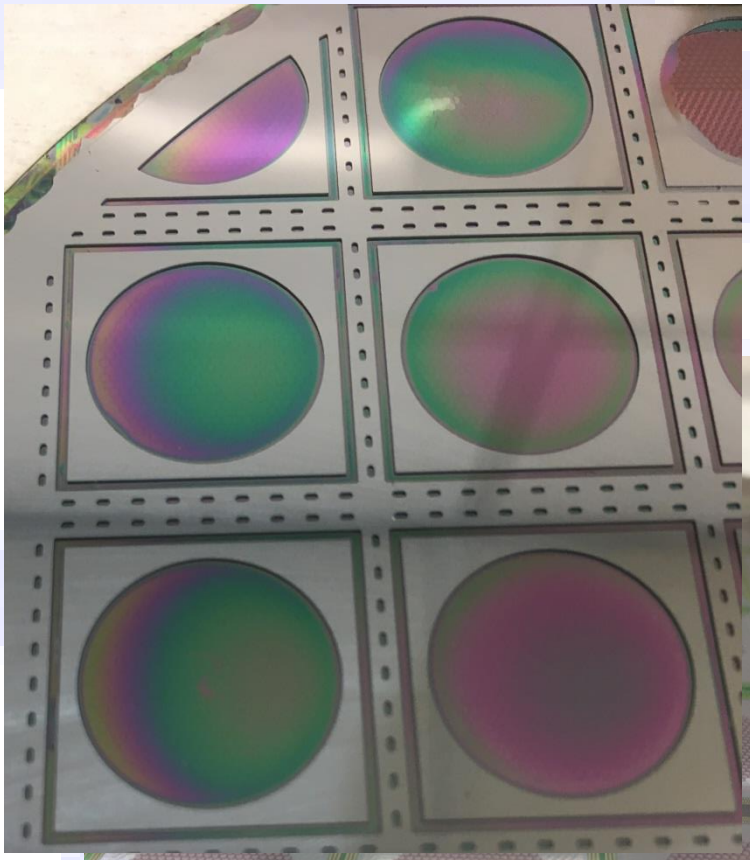
Phase II SBIR Development NNX14CG06C

Increasing Spatial Resolution (Increasing Yield)

PTT939: 1000-Actuator DM Fabrication

- Wafer-scale assembly developed
  - Multiple bondsite material stacks tested
  - Process complexity increased over multiple runs
- PTT939 Actuator and mirror wafer fabrication complete
- PTT939 wafer-scale assembly and etch to access mirror array completed
- 2nd wafer-scale assembly run to be completed Q1 2018
  - Reduce delamination
- Yield Increases
  - Projection lithography
    - Better uniformity
    - Excellent overlay error (layer-layer alignment)
    - 0 mask defects
  - Incorporate process improvements from PTT489 fabrication
    - Release development
    - Seed-layer etch improvements

PTT939 Bonded-Wafer Pair



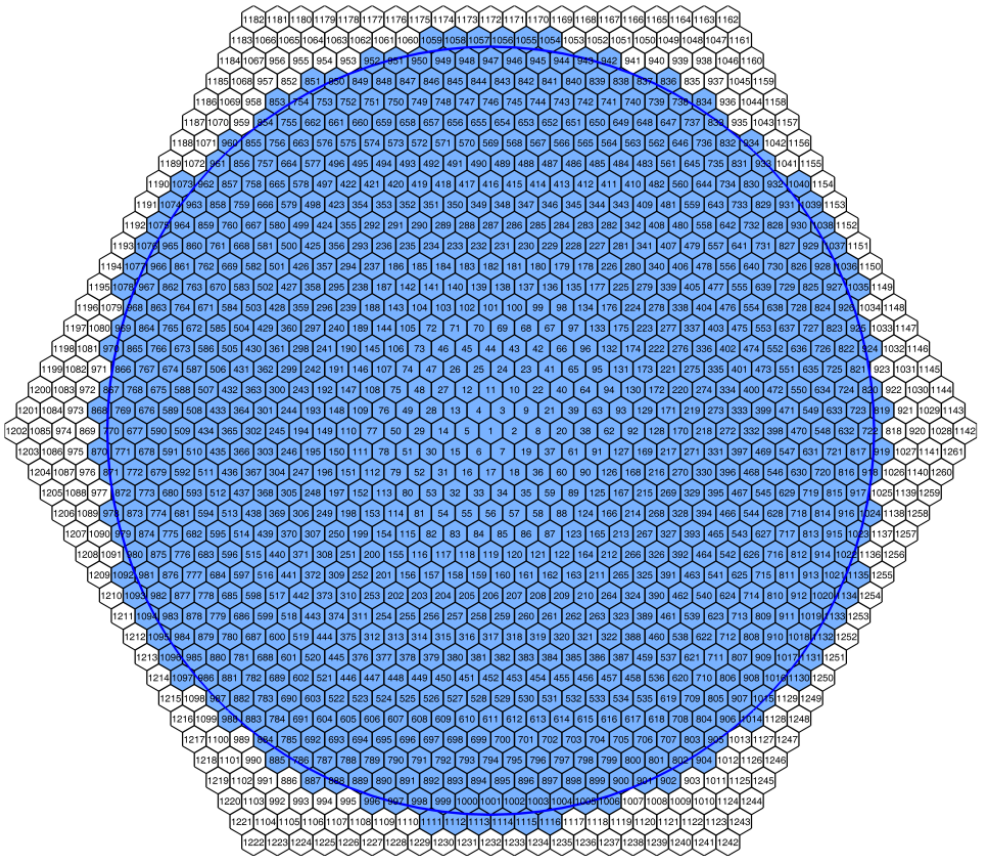
PTT939 Actuator Wafer

Phase I SBIR Development NNX16CD58P

Increasing Spatial Resolution Even More

Scaling to 3045 Actuators

- Design study of a 3045 actuator (1015 segment) DM
  - DM
  - Packaging
  - Electrical probe-testing hardware
- Results
  - All hardware is feasible using readily available technology
  - DM chip size: 35.6 mm x 27.4 mm
  - Field-stitching required for large arrays
    - Lithography system field size: 22mm x 27.4 mm
- Preliminary PTT3045 design and field-stitching completed in Phase I
- Yield study determined key source of defects in wiring layers
  - Process improvements resulted in 15X reduction in defects

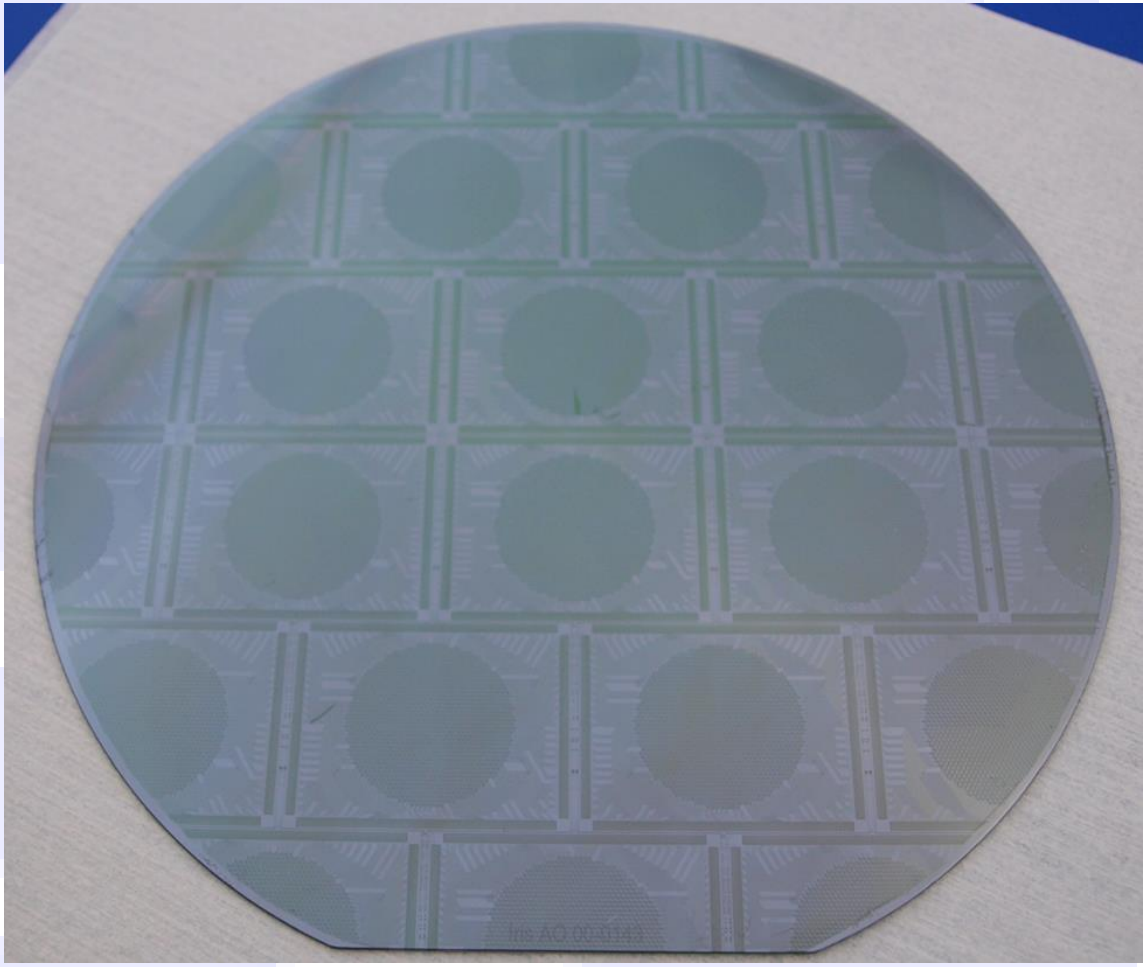


PTT3045 DM

- **3045 Actuators**
- **1015 PTT Segments**
- **19.6 mm inscribed aperture**

PTT3045 Field-Stitched Wiring Layer

- PTT3045 arrays are exposed in two halves: left and right
- Left/right field misalignment
  - 0.1 µm typical
  - 0.2 µm maximum
- Minimum feature size: 3.5 µm
  - 0.2 µm misalignment is inconsequential
- Phase I Conclusions
  - PTT3045 DM can be fabricated with proven/existing fabrication technologies
  - Scaling to larger arrays will require higher-density interconnect



Summary

- Super-resolution drive electronics demonstrated
  - Super-resolution technique shows clear increase in resolution: nearly 6+ bits
  - 30 minute stability
    - 19.6 bit stability with integrated 14 bit DAC/HV Amp chips
    - 17.7 bit stability with separate 16 bit DAC/HV Amp chips
- Wafer-scale assembly demonstrated
  - PTT939 (1000 actuator DM) fabrication nearly complete
  - Process improvements identified that will be implemented for 2nd assembly run
- 4th generation 3045 actuator DM technology assessment and preliminary design complete
  - Fabrication possible using existing technologies combined with field-stitching
  - Yield study reduced defects 15X