

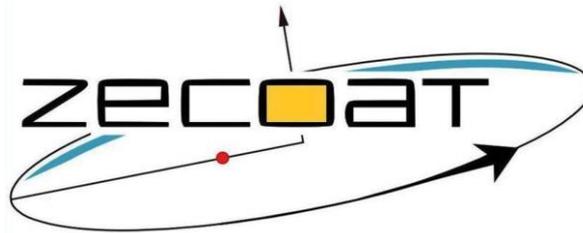
# Low-Stress Silicon Cladding for Surface Finishing Large UVOIR Mirrors NASA

(7<sup>th</sup> quarter status report)

SBIR Phase II contract No. NNX14CP14C

David Sheikh, Principle Investigator

David Redding (JPL), Technical Monitor



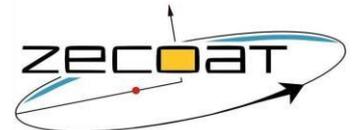
ZeCoat Corporation

Torrance, California

11/10/2015

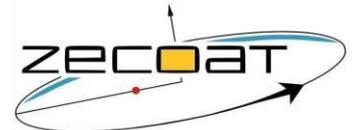
# Preview

- What is Si cladding?
- What are the goals of the Phase II research?
- What is the approach we've taken to develop a Si cladding process?
- What are the results of our efforts?
- What did we learn along the way?
- What are some possible applications for the Si product?



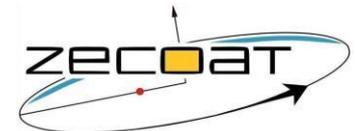
# What is Silicon Cladding?

- Silicon cladding is a material that may be applied on the surface of a SiC mirror substrate, to provide a better surface to polish and to reduce figuring time
- A 10 to 100-micron silicon layer is typically applied on top of the SiC
- Why Silicon? Good material to diamond turn or polish, and the CTE is very close to SiC



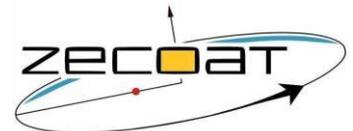
# Research Goals

- Create a viable Si cladding production process that meets the technical requirements for large and small mirrors
  - Developed moving source solution for large mirrors (greater than 1-meter in diameter)
  - Developed stationary source solution for smaller mirrors (less than 30-cm in diameter)
- Create a process that is scalable to very large sizes (~ 4+ meters)
  - ZeCoat's moving source Si process may be scaled to any size vacuum chamber.
- Create a process that is fast enough to be affordable for many applications
  - Small one-off mirrors require very high coating rates to keep cost reasonable



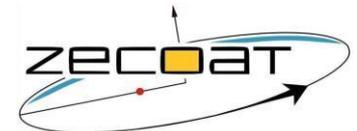
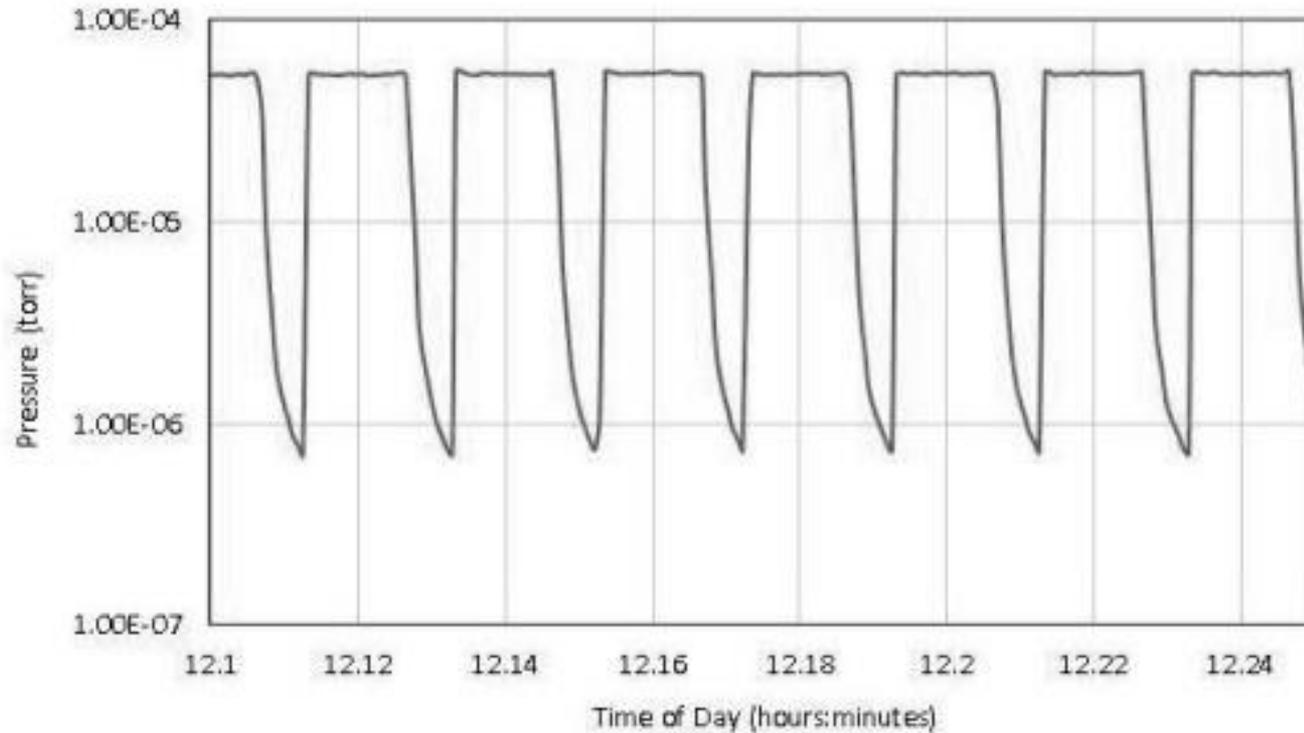
# Si cladding development history

In 2001, when making some dielectric mirror coatings on thin plastic membranes, I noticed that evaporated silicon films made with **argon ion bombardment** were *compressively* stressed, but contained *tensile* stress without bombardment.



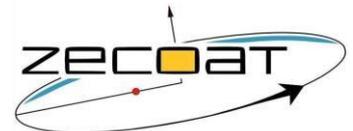
# Ion Pulse Automation

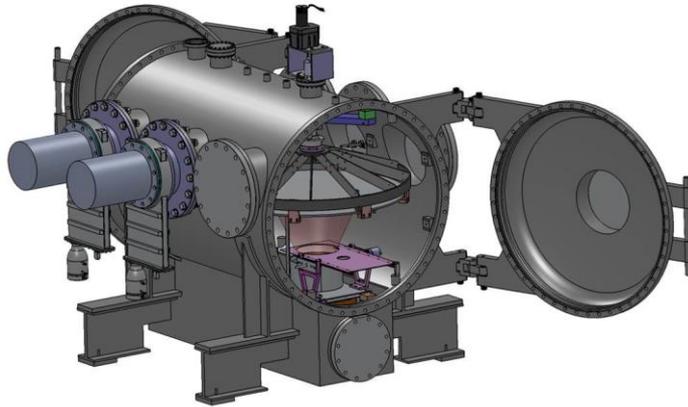
## Partial Pressure of Argon versus Time



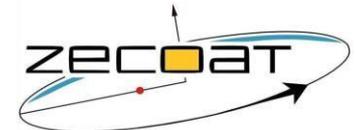
# Physical vapor deposition (PVD) of Si versus Chemical vapor deposition (CVD) (Si or SiC)

- CVD cladding is currently limited to smaller optics less than 1-meter
- Difficult and expensive to scale CVD processes up to large sizes greater than 2-meters
- Relatively high temperature process limits substrate compatibility (several hundred C versus ~80 C)

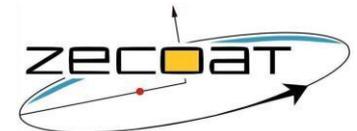
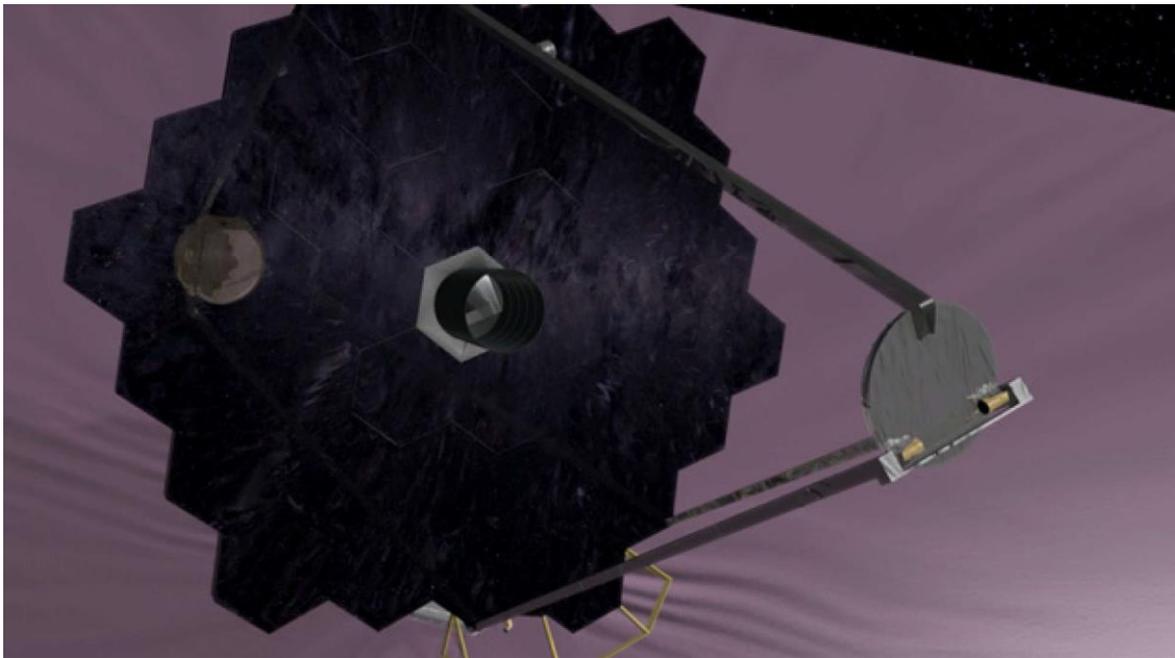




ZeCoat's 1.2-m vacuum coating chamber was completed in March, 2013 and utilizes an ion-assisted e-beam evaporation system

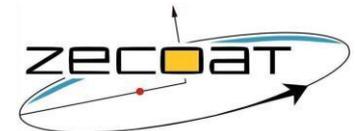


The goal of the Phase II research is to create a Si cladding process for finishing SiC mirrors for large segmented space telescopes (mirror segments in the 1.5-m to 2.5-m range).

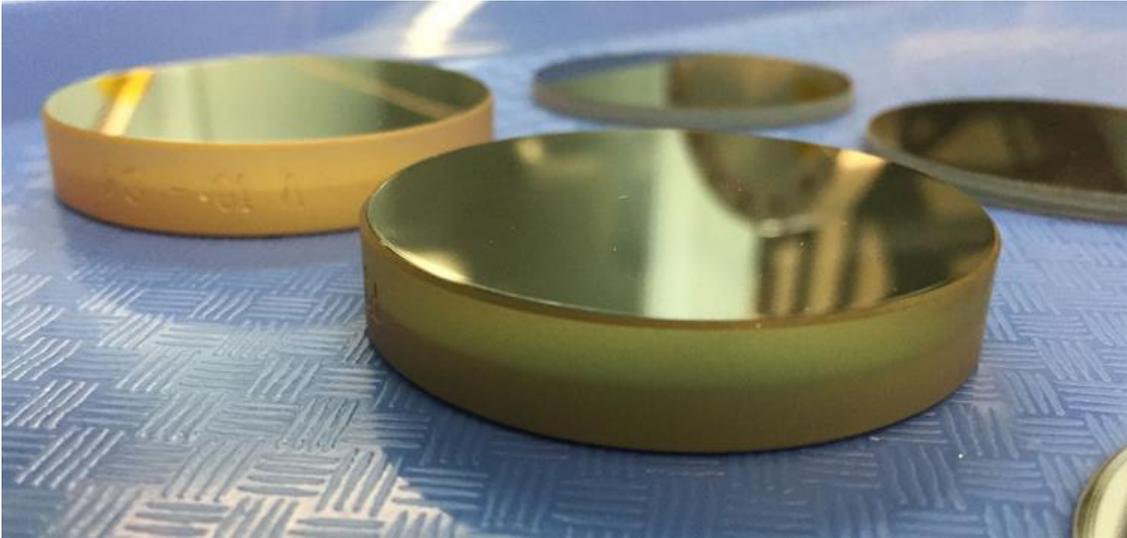


# Si Cladding Goals

	Future UVOIR Requirements	Visible Requirements (e.g. Kepler)	End of Phase I	End of 5 <sup>th</sup> Quarter of Phase II
Cladding Stress	< TBD (<85 MPa)?	NA	<85-MPa	<85-Mpa
Surface Roughness	< 5-angstroms RMS	< 20-angstroms RMS	3 to 30-angstroms RMS	< 3-angstroms RMS
Adhesion	Mil-tape adhesion test	Mil-tape adhesion test	Pass	Pass
Humidity	95%RH, 120F, 24-hrs	95%RH, 120F 24-hrs	Pass	Pass
Cladding Thickness	10 to 100-microns	NA	15-microns	44-microns
Scratch Dig	TBD	60/40	Very high	40/20

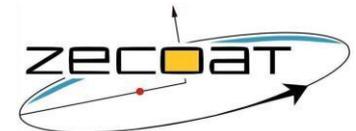


# Coating Stress and Polishing Results for Quarters 1-5



# Coating Stress Results (by quarter)

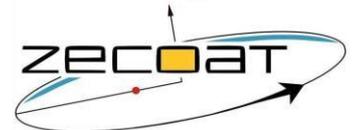
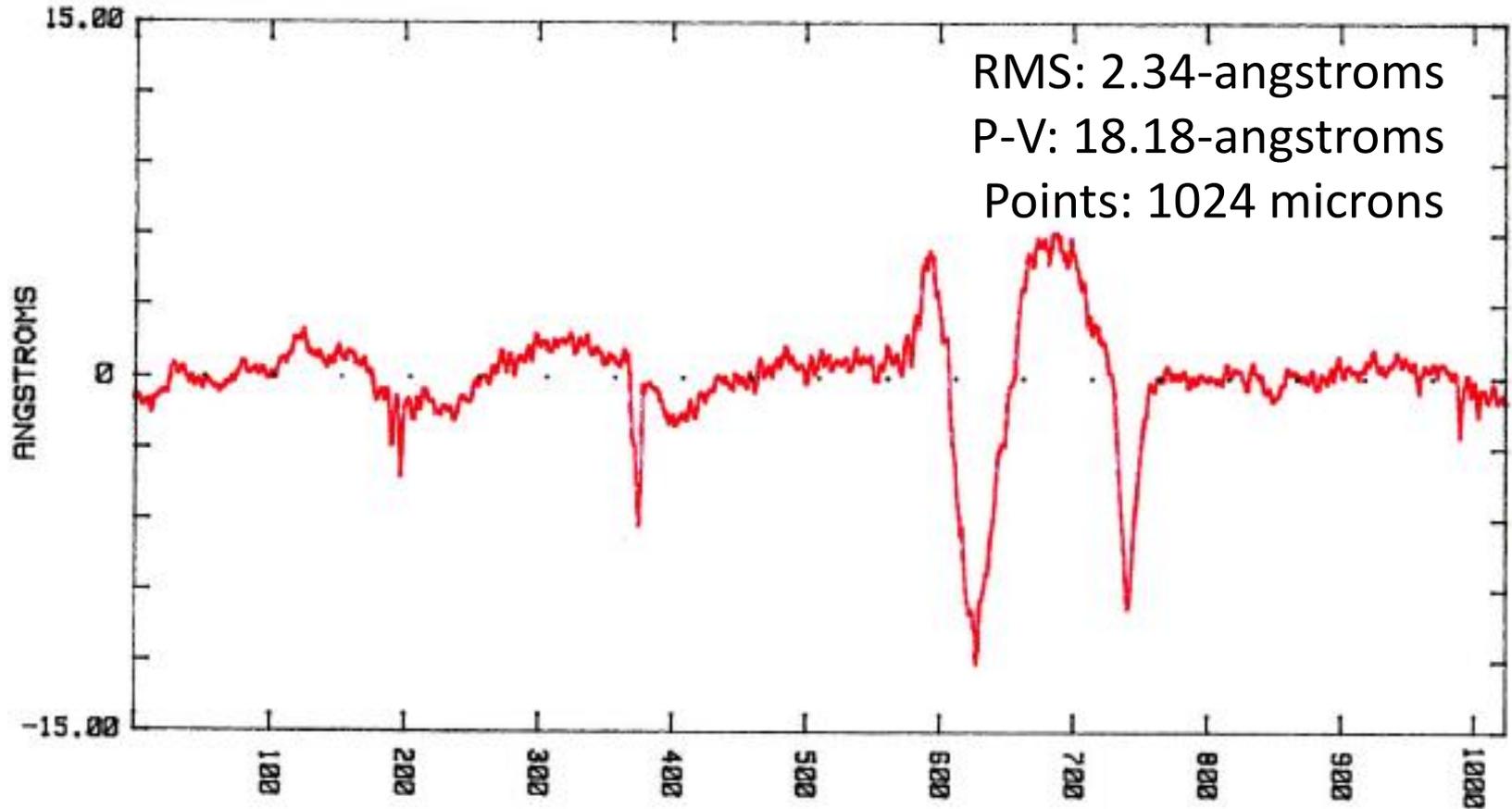
Period (quarters)	Silicon thick. (microns)	Goal (< +/- 85) Stress (MPa)	Sign
1st	NA	NA	NA
2nd	10	56	compressive
3rd	19	30	tensile
3rd	11	15	compressive
3rd	11	18	compressive
3rd	17	41	compressive
4th	44	84	compressive
5th	8	22	tensile
5th	20	51	tensile



# Polishing Results

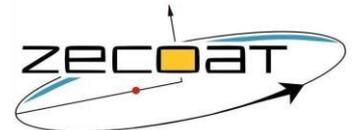
Sample ID	measurement #	Before Polishing		After Polishing	
		RMS (A)	PTV (A)	RMS (A)	PTV (A)
464 (high evap rate)	1	16.61	363.18	1.06	9.94
464 (high evap rate)	2	10.65	132.43	2.34	18.18
464 (high evap rate)	3	21.48	454.77	0.5	6.11
464 (high evap rate)	4	34.22	618.42	0.4	2.6
464 (high evap rate)	5	12.87	185.14	0.74	7.09
464 (high evap rate)	6	20.88	501.61	0.74	8.51
464 (high evap rate)	7	12.74	220.19	0.72	6.88
464 (high evap rate)	8	10.67	118.21	0.79	4.79
464 (high evap rate)	9	18.78	317.66	0.65	3.54
464 (high evap rate)	10	11.11	111.85	0.7	3.66
<b>average</b>		<b>17.00</b>	<b>302.35</b>	<b>0.86</b>	<b>7.13</b>
469 (low evap rate)	1	9.95	65.23	2.55	15.47
469 (low evap rate)	2	13.33	246.83	0.66	3.83
469 (low evap rate)	3	9.23	67.64	1.17	7.53
469 (low evap rate)	4	9.34	61.14	2.63	14.59
469 (low evap rate)	5	8.48	53.83	1.09	6.87
469 (low evap rate)	6	8.42	51.26	1.07	5.56
469 (low evap rate)	7	8.93	73.86	2.82	13.71
469 (low evap rate)	8	9.64	69.11	1.11	8.9
469 (low evap rate)	9	29.19	684.12	0.67	4.23
469 (low evap rate)	10	8.33	51.96	0.77	8.1
<b>average</b>		<b>11.48</b>	<b>142.50</b>	<b>1.45</b>	<b>8.88</b>

# Measurement of surface micro-roughness



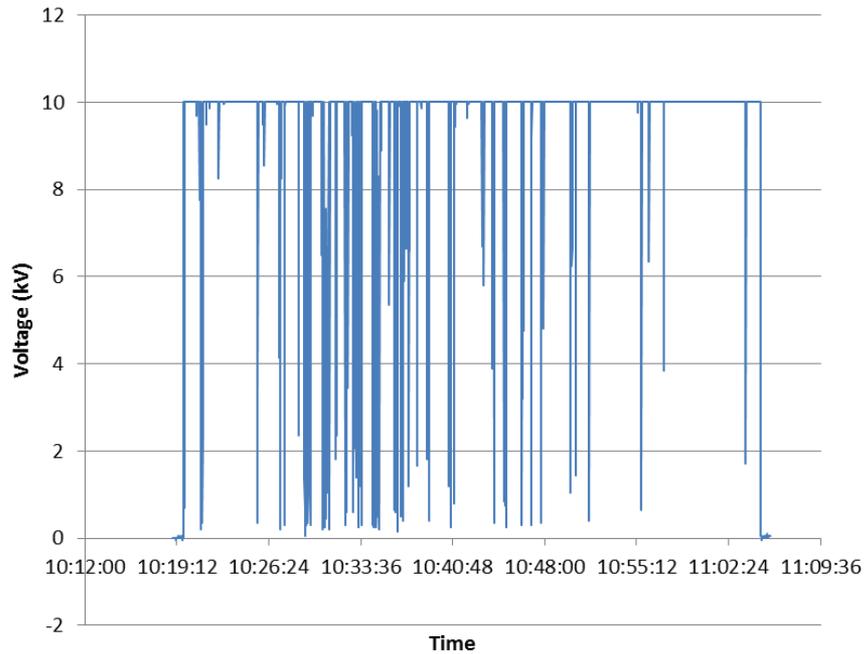
# Phase II challenges and what did we learn?

- Investigated resistive evaporation as alternative to e-beam evaporation
  - Learned that silicon splashes out of liner at relatively low rates
  - Excessive heat causes outgassing and Si contamination
  - Lots of engineering challenges to solve but its certainly possible
- Electrical arcing during e-beam process
  - Modified the chamber to make it impervious to arcing events
  - Created method to monitor arc frequency, duration and magnitude
  - Learned that severe arcing causes defects in coating when e-beam strikes the evaporation crucible
- Surface defects
  - Dust contamination
  - Raw silicon materials “spitting”
  - E-beam missing target material
- Coating rates
  - Increased evaporation rate by optimizing ion current
  - Si deposition rate increased by a factor of 6x!!!

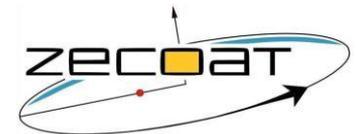
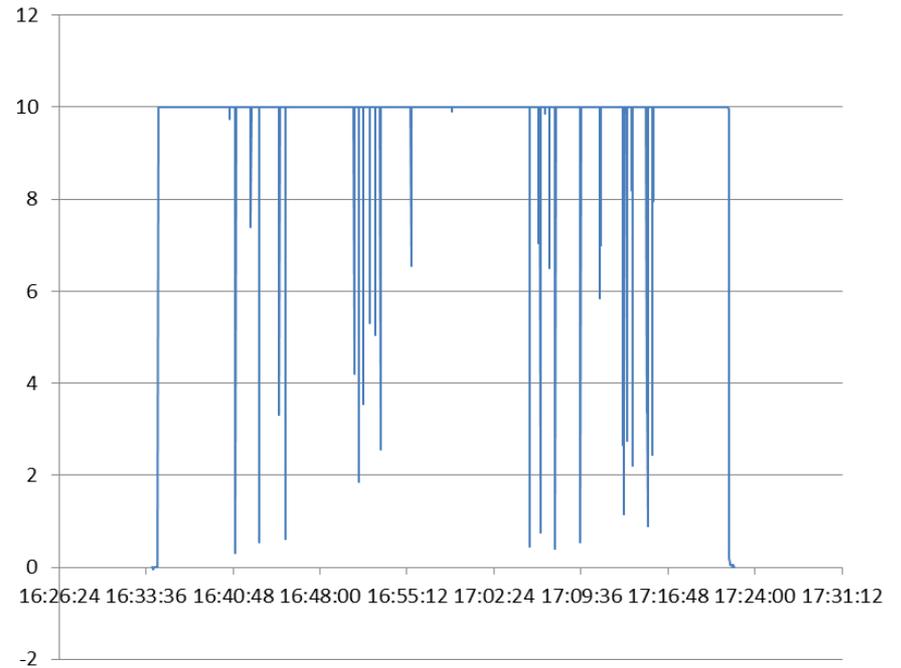


# Electrical arcing

Voltage drop-outs during coating run from arcing



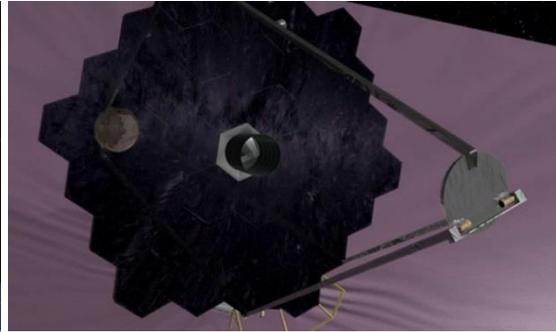
Voltage drop-outs during coating run from arcing



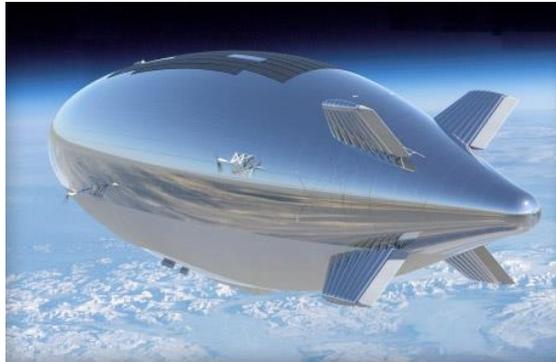
# Applications for Si Cladding



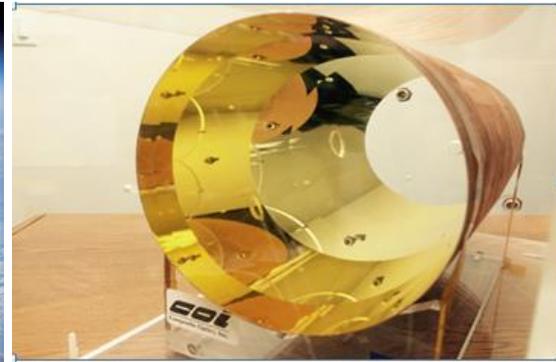
**a. RF Reflectors**



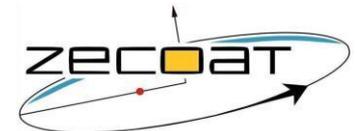
**b. Lightweight mirrors**



**c. Thin film solar cells**

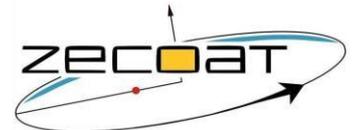


**d. X-ray optics**



# Conclusion

- ZeCoat has developed a low stress silicon cladding based on a low temperature process suitable for application to plastics, SiC, etc.
- ZeCoat's current processing chamber can coat mirrors up to 1.15-meters in diameter and the process is scalable to larger mirrors in excess of 2-meters
- Si cladding process rates are up to 6x faster than 1-year ago making the product much ~~more affordable~~ higher profit! 😊



# Questions?

