MEMS Deformable Mirror Development for Space-Based Exoplanet Detection

Iris AO, Inc.

NASA Phase II SBIR: NNX11CE94P
NASA Phase II SBIR: NNX14CG06C

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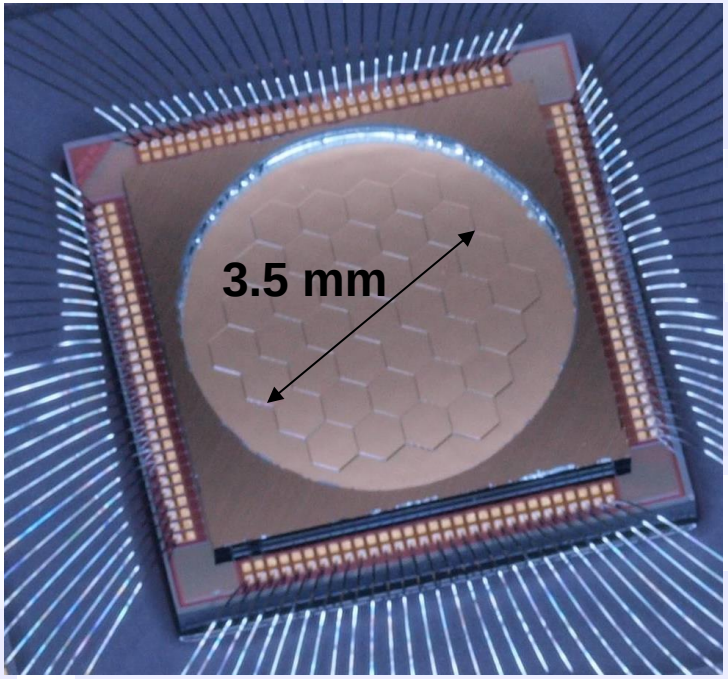
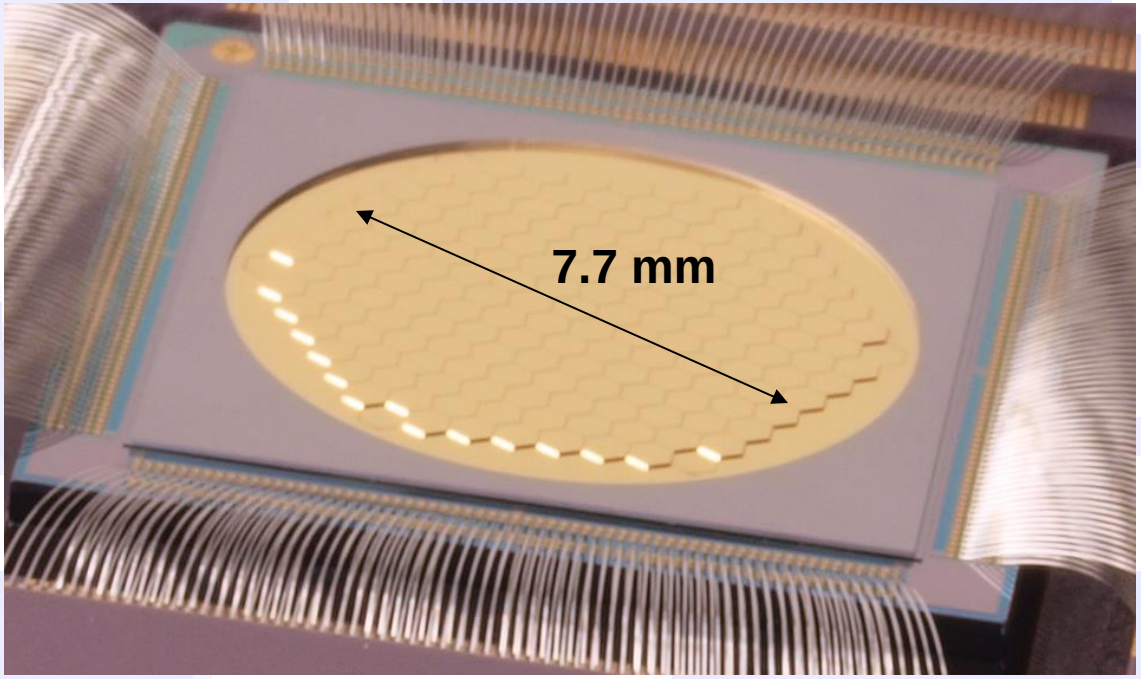
Iris AO Segmented DM Background

Iris AO MEMS Segmented Deformable Mirrors

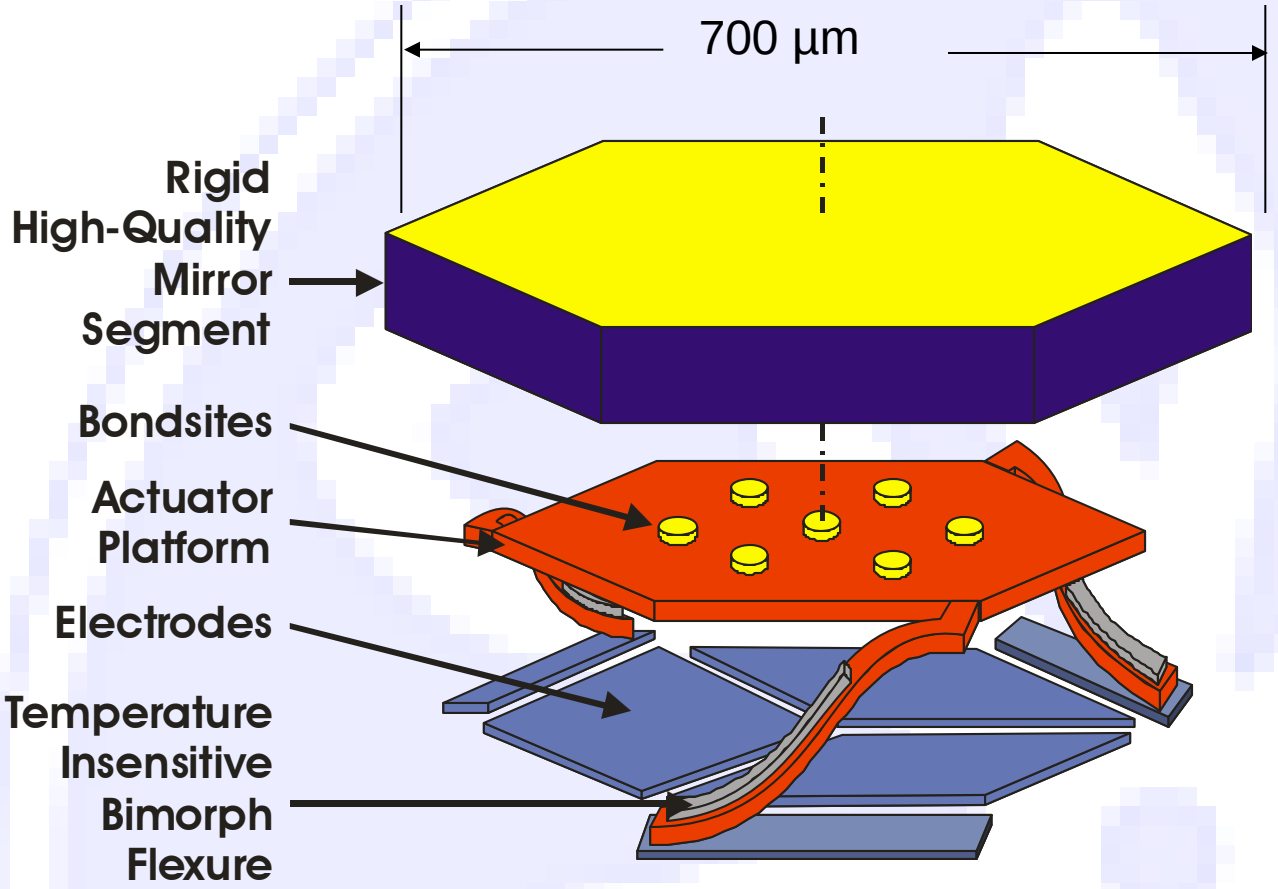




PTT111 DM
- 111 Actuators
- 37 PTT Segments
- 3.5 mm inscribed aperture
- Factory calibrated

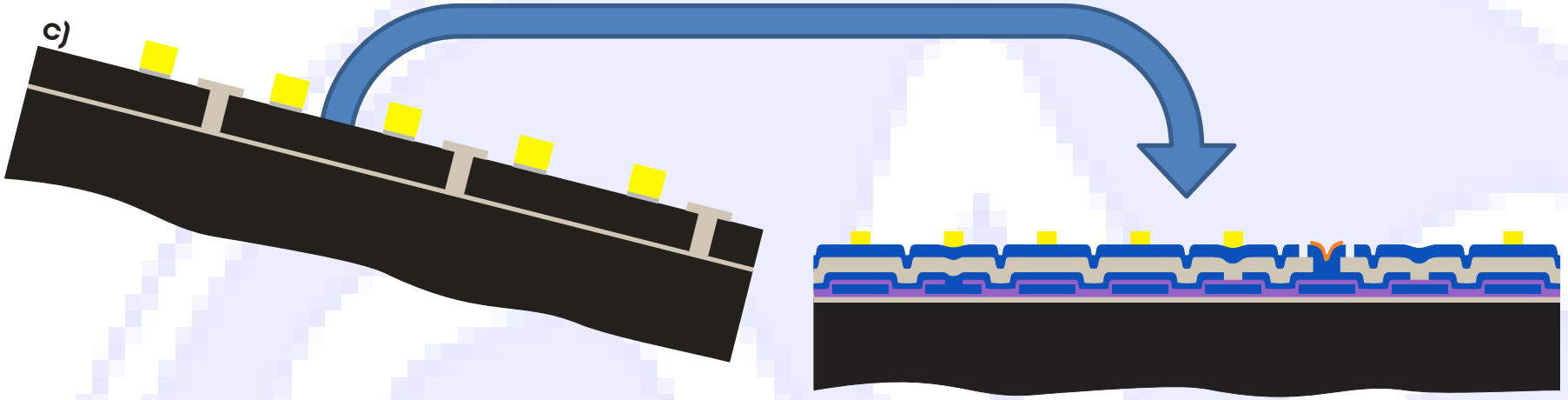
PTT489 DM
- 489 Actuators
- 163 PTT Segments
- 7.7 mm inscribed aperture
- Factory calibrated

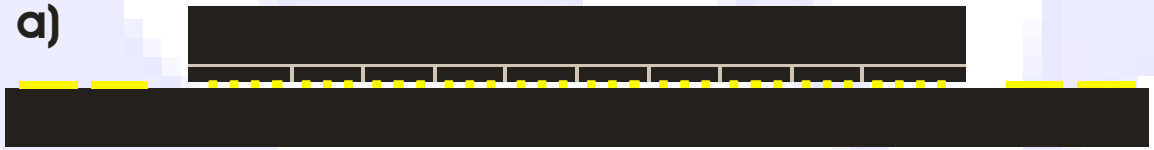
Iris AO Segmented DM Background



- 3 DOF: Piston/tip/tilt electrostatic actuation – no hysteresis
- Hybrid fabrication process
  - 3-layer polysilicon surface micromachining
  - Single-crystal-silicon assembled mirror
- Unit cell easily tiled to create large arrays
- Hybrid technology
  - Thick mirror segments
  - <1 nm PV/°C segment bow
  - Enables back-side stress-compensation coatings

Hybrid Fabrication Process





Chip-scale thermo-compresion flip-chip bond

Mirror-aperture clearing etch

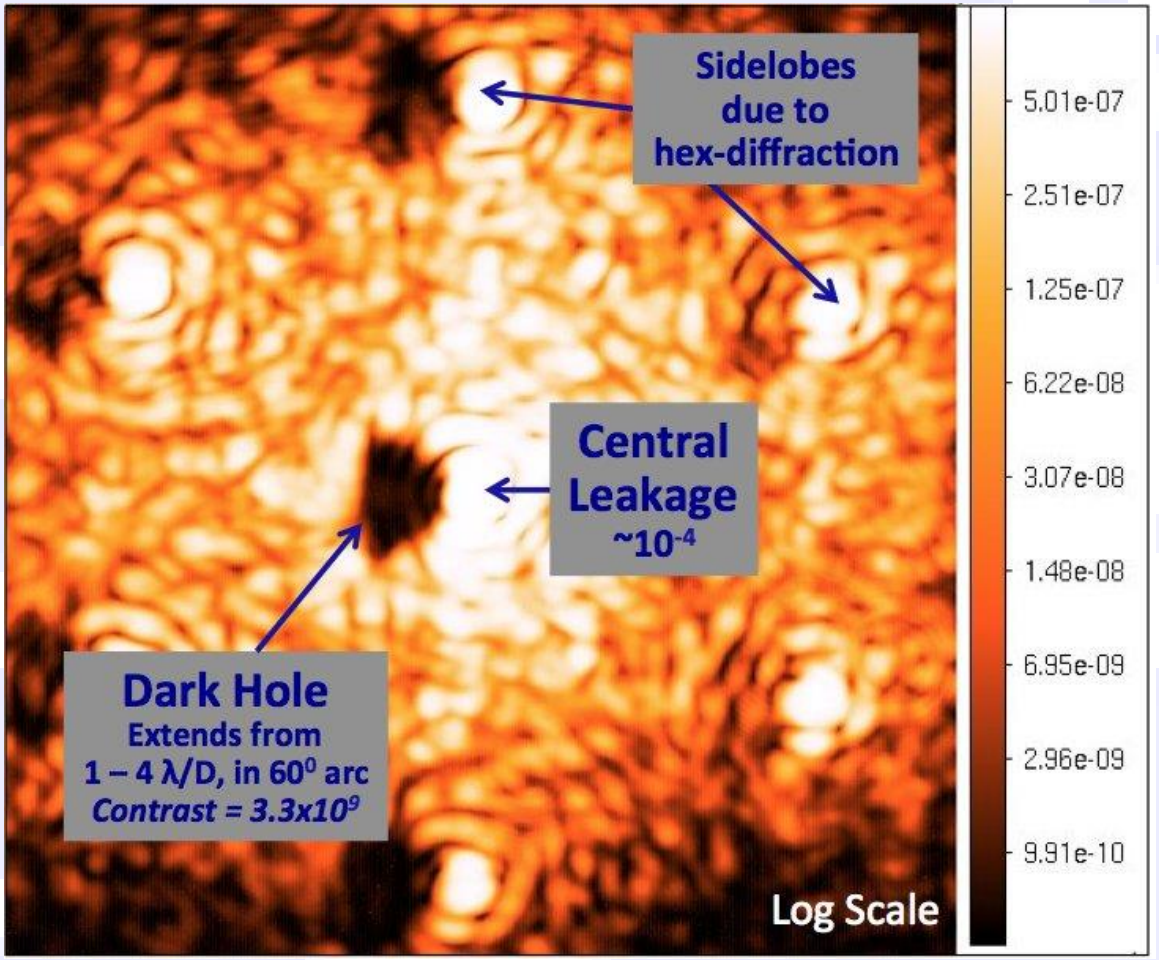
Microstructure release and optical coating

NASA Application

Visible Nulling Coronagraph (VNC)

Exoplanet Imaging Requirements: VNC Technology

- Usable Dynamic Range (Stroke): 1.0 µm
- Segment Control Resolution: 15 pm *rms*
  - ATLAST: may now be 1 pm *rms*
- ~1000 Segment DM
- Segment Flatness: 1-3 nm *rms*



10⁹ Contrast @ IWA 1 – 4 λ/D Results GSFC VNC Instrument on 06/09/12

R.G. Lyon, M. Clampin, P. Petrone, U. Mallik, T. Madison, M.R. Bolcar, "High Contrast Vacuum Nuller Testbed (VNT) Contrast, Performance and Null Control," Proc. of SPIE 8442 (2012).

Phase II SBIR Development

Critical Development for Manufacturing DMs for Exoplanet Detection

Phase II Objectives

NNX11CE94P

- Improve DM quality
  - Improve segment flatness for entire array
  - Reduce chip bow
  - Increase segment position uniformity
- Scale technology to 1000-actuator DM
  - Increase yield
  - Demonstrate PTT939 array
- Demonstrate pm-level positioning
  - 15 pm rms

NNX14CG06C

- Wafer Scale DM Assembly
- 16 Bit Electronics
- Hardware-based super resolution electronics controller

Mirror-Segment-Flatness Improvements

Segment Design	Average *rms* Errors	Worst *rms* Errors
25 µm	12	22
50 µm	3	4.5
50 µm (400 µm Aperture)	*1.5 (1.1, best result)*	*2.1*
25 µm Optimized	5	8
50 µm Optimized	NA	NA

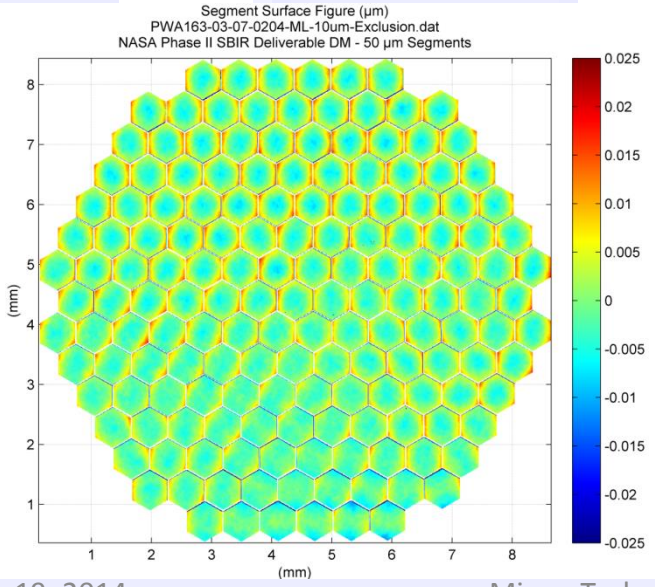
Matches 1st Order Theory Well: 4X reduction for 50 µm vs. 25 µm segments

Phase II Goal: 2 nm *rms*

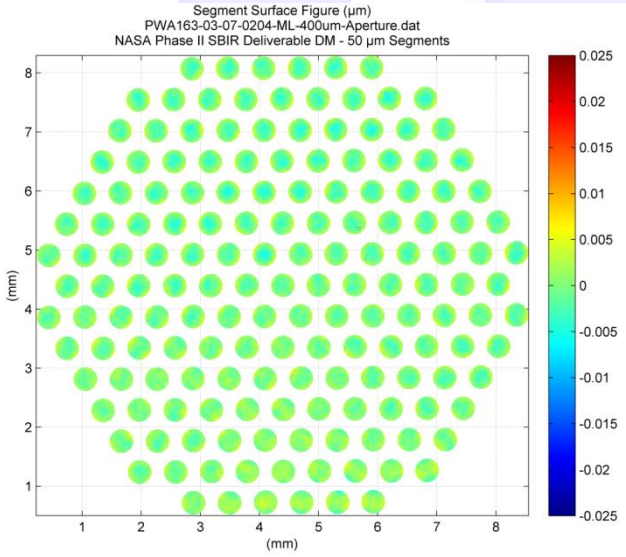
If trends hold, ~1.25 nm *rms* over entire segment should be possible

50 µm-Thick DM Segments - Phase II Deliverable

Full Aperture (10 µm Exclusion)

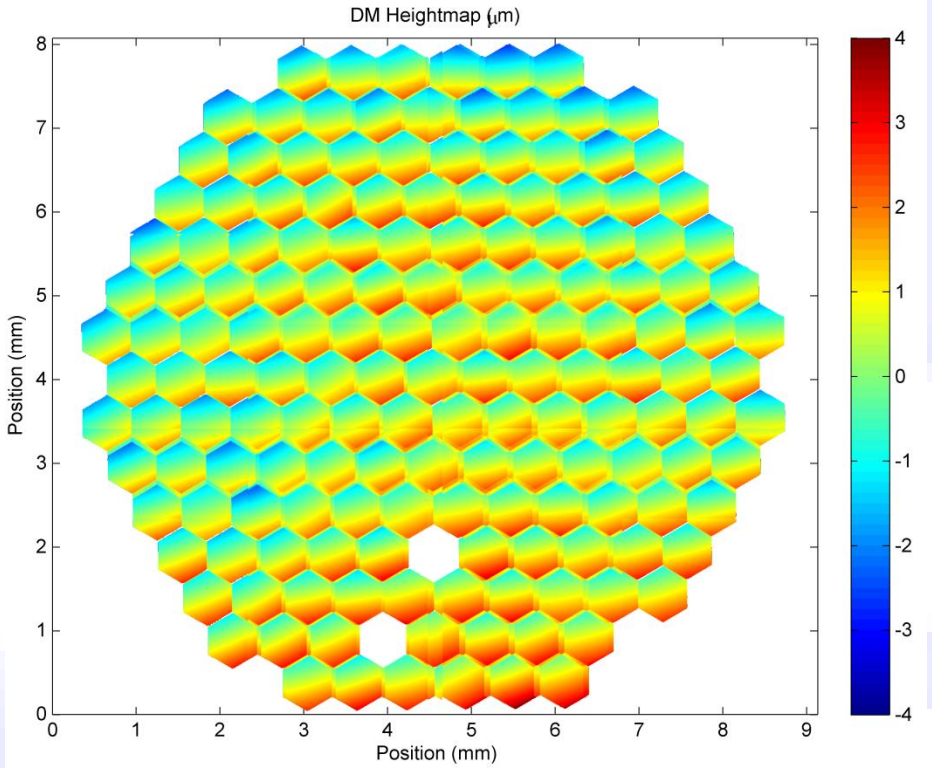


Partial Aperture (400 µm Aperture)

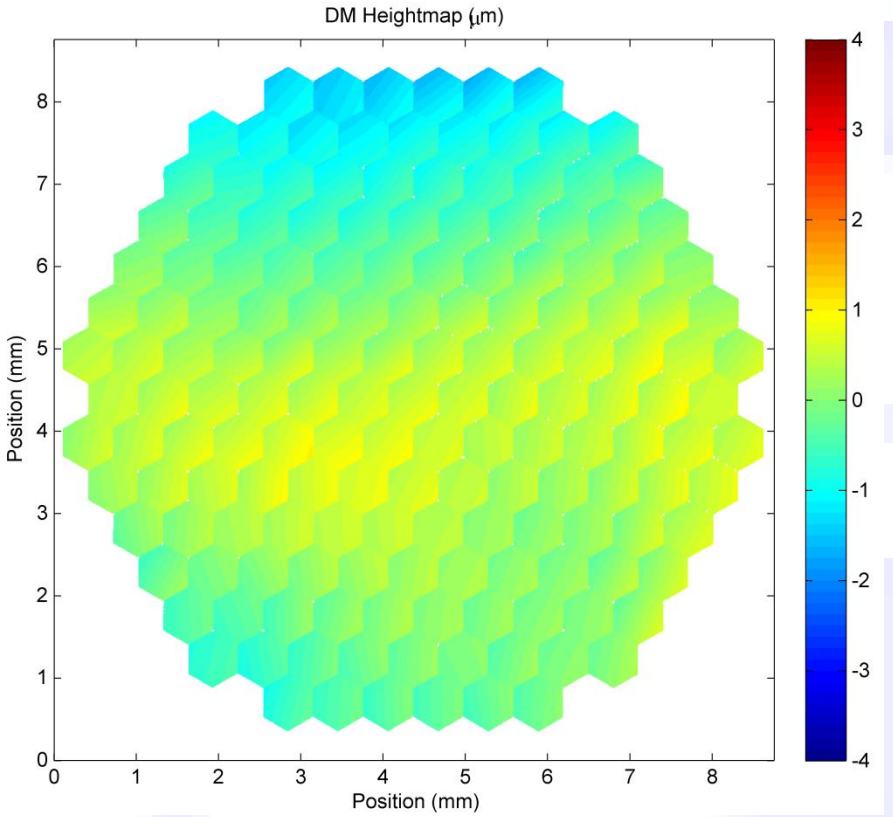


Unpowered DM Figure Improvement

Unpowered PTT489 DM



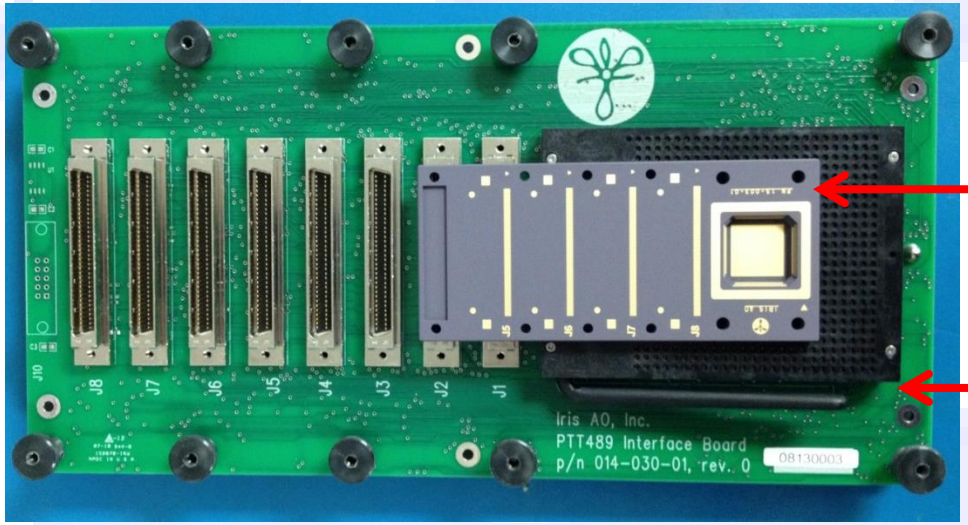
Pre Phase II



Phase II Interim Deliverable

DM Packaging Improvements

- Reduced mass
  - 1.26 kg → 0.34 kg
- Reduced footprint
  - 5”x10” → 2”x5.5”
- Increased Thermal Stability (nm PV/°C)
  - 12.5 → 3.5



2nd Generation LGA Package

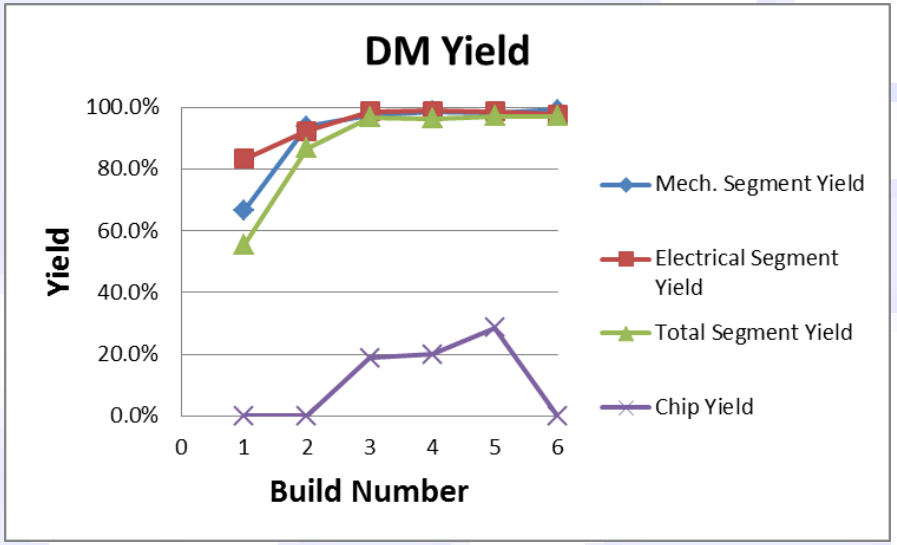
1st Generation PGA Mirror Interface Board

PTT489 - PGA		
Description	Weight (oz)	Mass (kg)
PGA Package	1.9	0.05
MIB PCB	13.0	0.37
Mounting Block	29.6	0.84
Total (summed)	44.5	1.26
Total (measured)	44.5	1.26

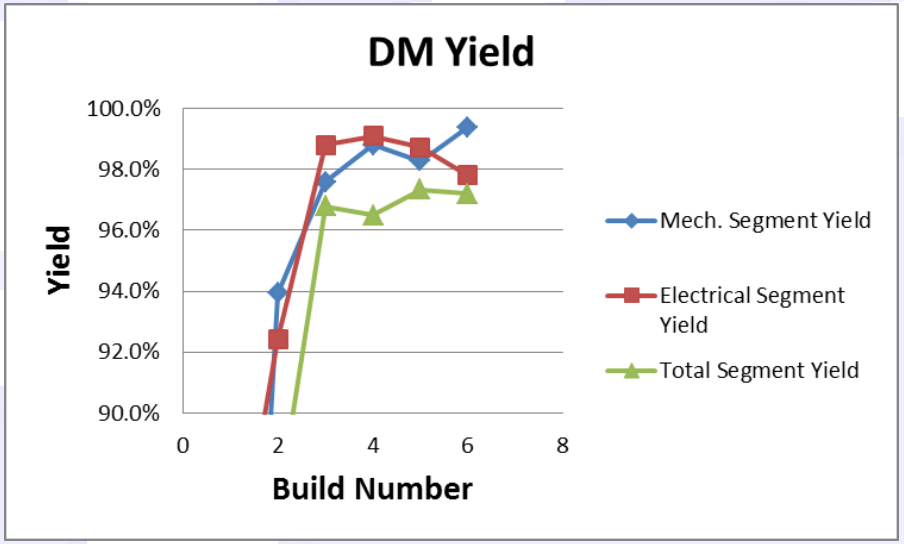
PTT489 - Compact LGA		
Description	Weight (oz)	Mass (kg)
LGA Package	3.0	0.09
Enclosure Top	2.5	0.07
Enclosure Base	3	0.09
Mounting Bracket	3.2	0.09
Total (summed)	11.7	0.33
Total (measured)	11.8	0.34

DM Yield

DM Build Number	Actuator Wafer Lot	Mirror Wafer Lot	Mech. Segment Yield	Electrical Segment Yield	Total Segment Yield	Chip Yield
1	PWA-02	LSM-01	66.8%	83.4%	55.7%	0.0%
2	PWA-02	LSM-02	93.9%	92.4%	86.8%	0.0%
3	PWA-03	LSM-02	97.6%	98.8%	96.8%	18.8%
4	PWA-03	LSM-02	98.8%	99.1%	96.5%	20.0%
5	PWA-03	LSM-02	98.3%	98.7%	97.3%	28.6%
6	PWA-04	LSM-02	99.4%	97.8%	97.2%	0.0%
7	PWA-05	LSM-03	TBD	TBD	TBD	TBD

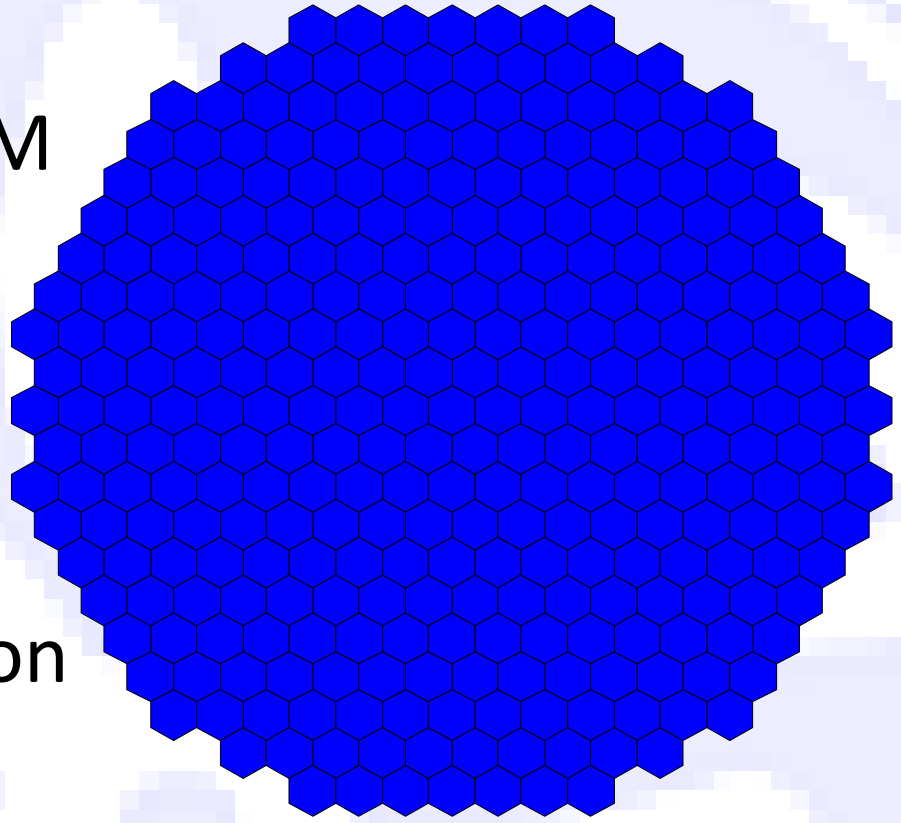


- Ideally yield increases monotonically with every fabrication lot
- Defects in contact masks increased electrical failures for PWA-04 actuator lot
  - Defects were more uniformly distributed rather than clustered
  - Result: 0% chip yield
- Goal: fully functional PTT939 DM
- PWA-05 Run
  - New masks
- PTT939 DM will used DUV stepper photolithography
  - Fewer defects from lithography



NASA Phase II SBIR: Remaining Work

- NNX11CE94P
- Demonstrate PTT939 DM
  - Transition fabrication process to DUV stepper lithography system
- Demonstrate mass-reduced DM segments on a PTT489
  - Phase IIE



PTT939 DM
10.85 mm aperture
313 PTT segments
939 actuators

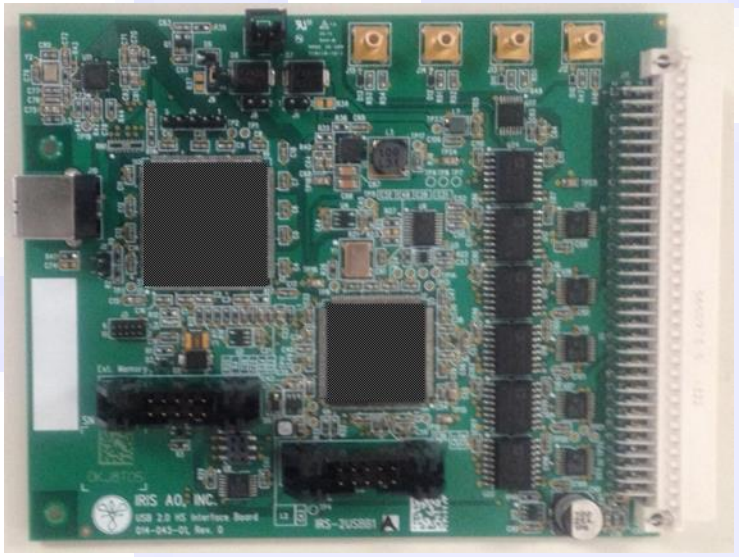
Electronics Development

- Existing Iris AO Drive Electronics are 14-bit resolution

NNX14CG06C Development

- 16-bit resolution HV driver card
  - Card built and preliminarily tested

- USB2.0 High Speed Interface
  - Microcontroller
  - FPGA to implement timing critical modulation
  - Windows and Linux compatible
  - Built, tested, and currently being incorporated into Iris AO interface software

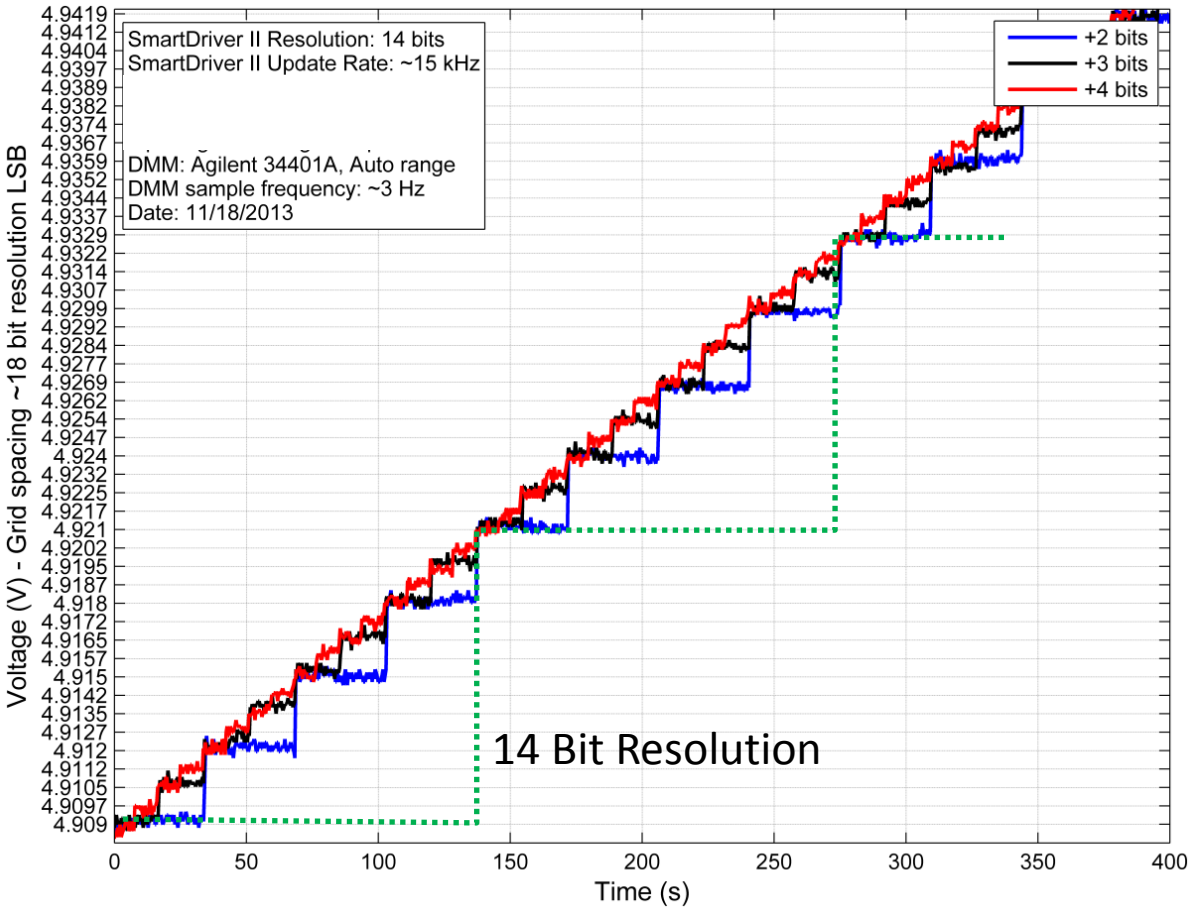


High-Resolution Drive Electronics

- pm *rms* level control will require >20 bit electronics
  - 2 µm stroke DM, 1 µm stroke after flattening
  - Nonlinearity in MEMS electrostatic actuation reduces resolution
- State-of-the art HV MEMS Drivers are 14-16 bit resolution
- Signal processing techniques can be used to increase resolution (super resolution)
  - NASA New Technology Report to be filed

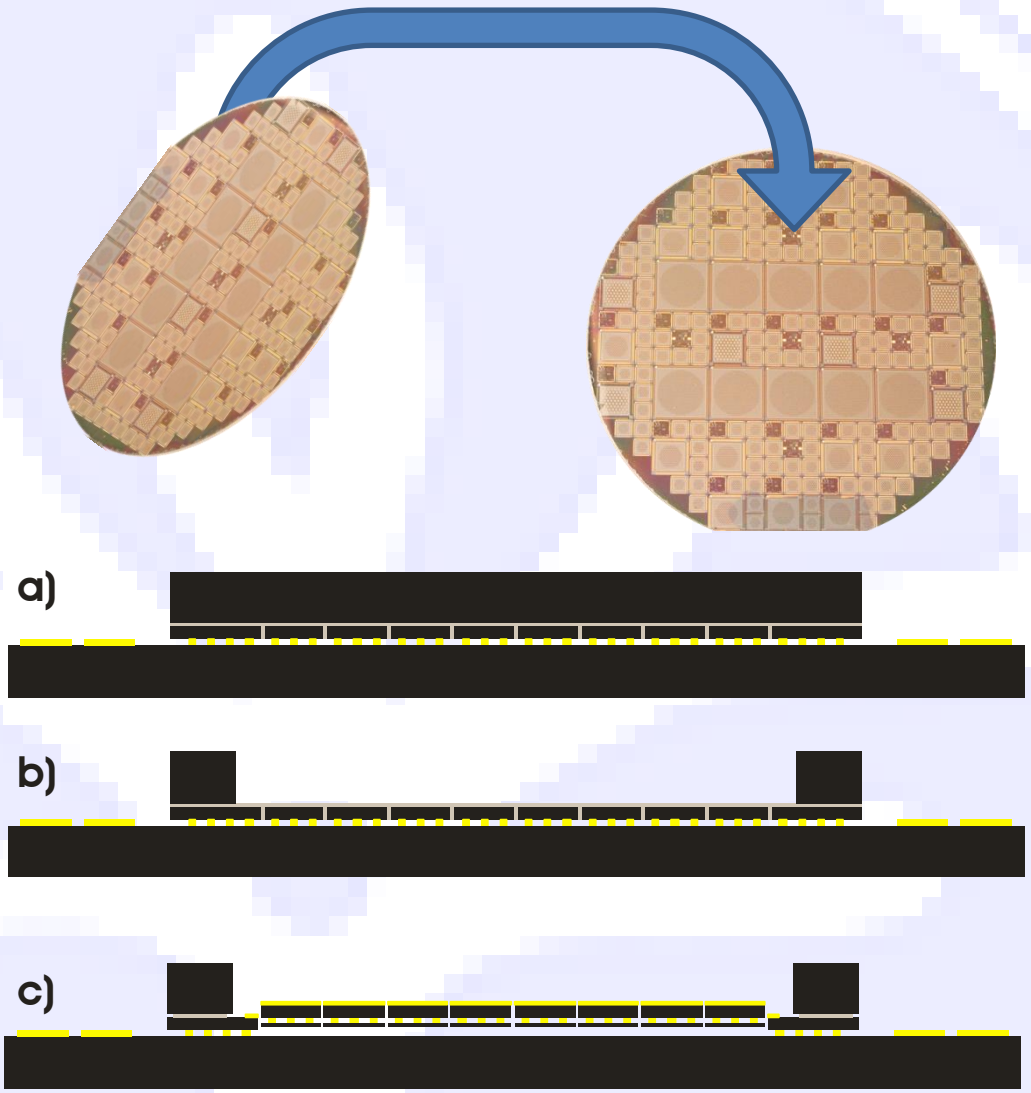
Super-Resolution Drive Electronics

- Electronics are 14 bit resolution
- Grid spacing is for 1 LSB on 18 bit resolution
- Super-resolution demonstration
  - +4 bits were demonstrated
- FPGA controlled signals will provide even better resolution



Scaling Up: *Wafer-Scale Assembly*

- DMs >1000 actuators require wafer-scaled assembly techniques
- Phase I demonstrate a scalable bonding technique using a eutectic bond
- Recent increased bond-tool tool capacity and process optimization enables wafer-scale thermo-compression
  - gives a lower risk path to wafer-scale assembly
- Eutectic bond will be developed as a back up plan



Summary

Technologies developed to produce DMs capable of meeting VNC requirements

- Segment flatness 2nm *rms* over VNC subapertures
  - Path to flatter segments
- Segment position variations reduced to suitable levels for testbed environment
- Compact, more thermally stable packaging
- Major yield improvements
  - Defects on recent PEA-04 run determined
  - Higher yields expected on PWA-05 run
- Demonstrated means to reach 20 bit drive electronics resolution
- Wafer-scale assembly under development
  - Enables scaling to 4th generation 1000 segment (3000 actuator) DM
- Design of 3rd generation 1000 actuator DM underway