Small Satellites Demand Innovation in Reliability
Harald Schone, JPL
Huygens probe lands on Saturn on this day, Jan 14 2005

What's Wrong with SmallSat Reliability?

- A few basic truths:
  - More experienced institutions are more successful
  - Over the decades more missions succeed
  - Mission capabilities have vastly improved
- 4 things you like when developing reliable SmallSats
  - … experienced engineers
  - … a multi-discipline team
  - … plenty of money and schedule
  - … have learned to deal with COTS

What to do if you don't have all "4"?

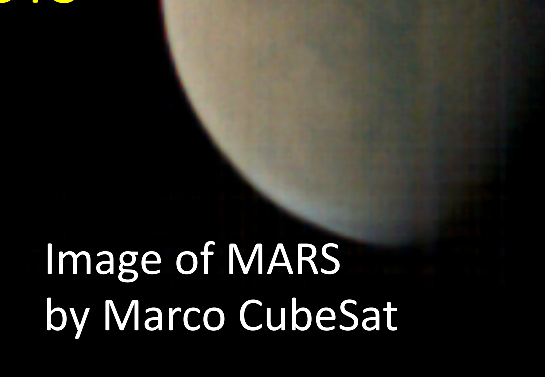
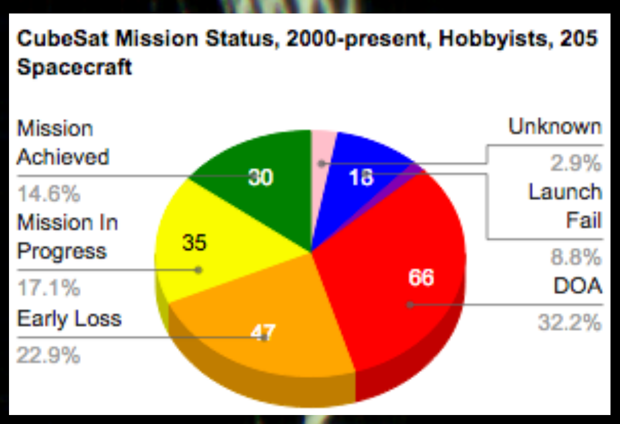
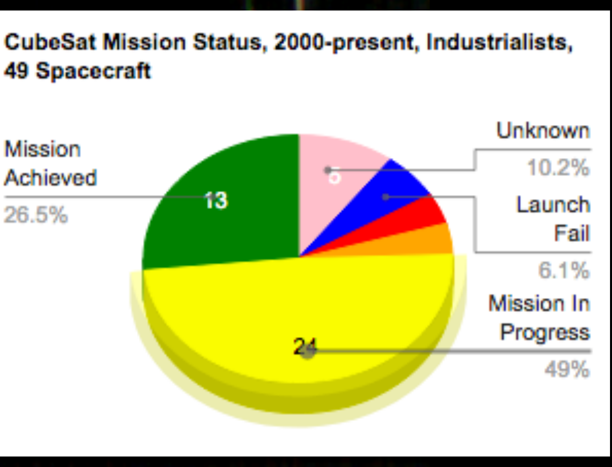


Image of MARS
by Marco CubeSat





Michael Swartwout

Reliability in CubeSats is Challenging

- Small form factor and low power demands COTS electronics
  - Long term reliability not an issue
  - Radiation effects are a major concern, specially for non-LEO missions
  - Typically no radiation data exists for COTS
- Tremendous variation in missions types- every cubesat is a unique
  - Risk posture, duration, environment, schedule, cost, complexity, …
- Huge variation in each institution's knowledge base
  - A one-size-fits-all training is ineffective

We established the Small Satellite Reliability Initiative as an answer to these challenges

Goal 1: Innovate Sharing Knowledge

- Effective knowledge sharing requires thought
  - Effective ways to collect information: Useful/Complete/ Quick
  - Find formats to facilitate information sharing
    - Sharing piles of papers, seminars, lists of lessons learned or best practices is cumbersome and discourages adoption
  - How to best navigate through this information (standard format & metadata)
  - Guide you through a design/development/Ops process?- Expert System
  - Do you want to be predictive?- Share models
- Make use of vague information. Example:
  - “generally this part has a low TID tolerance” ✓
  - ….use CMOS with feature sizes <45nm ✓
  - … the parts are susceptible to SEL ✓
  - Design for simplicity

Overview of Workshop Results: Communicating Risk

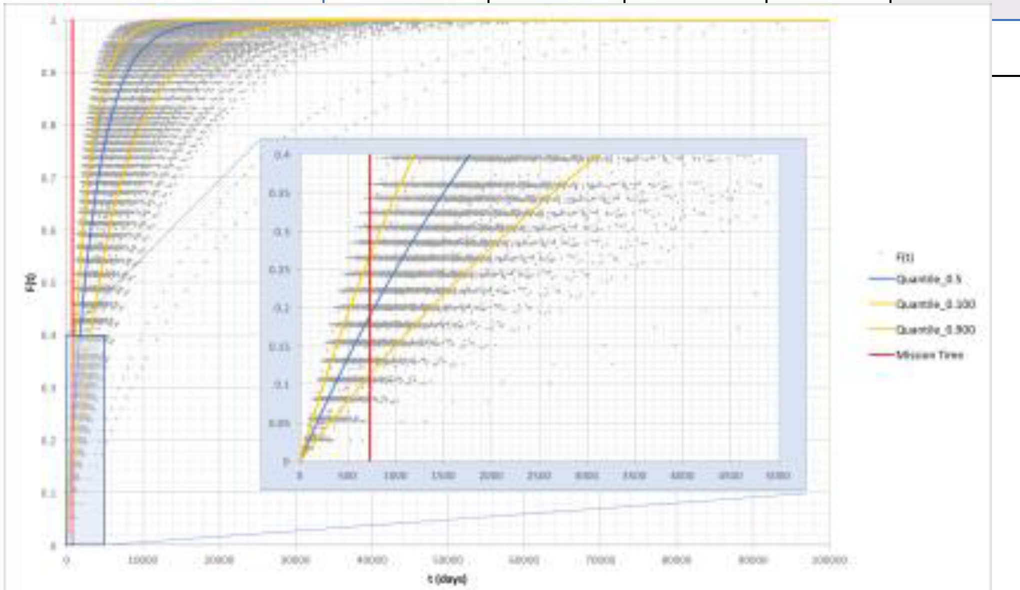
- Tailoring Matrices
  - Classify & communicate risk
  - A subgroup is developing characteristics for a number of mission ‘types’ that impact reliability
  - Risk mitigation binned by risk posture
  - Governance tailored by risk tolerance
- Risk Models
  - System level libraries under development
  - Studies system architecture and fault protection
  - Informs sponsor of key risk drivers

Mission characteristics for an LEO/GEO Mission

Risk Tolerance → Mission Characteristics ↓	Very Low	Low	Moderate	High	Very High
Mission Criticality	National Security; Operational	Operational; Primary Science	Gap Filler	Experimental; Technology Demo	Technology Demo; Teaching System
LEO Mission Life	5+ years	3-5 years	~1 year	Months	Days to weeks
GEO/Deep Space Mission Life	10+ years	5+ years	1-3 years	Months	Days
					Technology Demonstration
		High unit cost;			Re-launch readily available
					<12 months

Mission characteristic for a large constellation

Risk Tolerance → Mission Characteristics ↓	Very Low	Low	Moderate	High	Very High
Mission Criticality	National Security; Operational	Operational; Primary Science	Gap Filler	Experimental; Technology Demo	Technology Demo; Teaching System
LEO Mission Life	5+ years	3-5 years	~1 year	Months	Days to weeks
GEO/Deep Space Mission Life	10+ years	5+ years	1-3 years	Months	Days
Single Satellite	Operational Mission	Data gathering	Gap Filler	Experiment	Technology Demonstration
Constellation (>10) Satellites	Common mode failures ruled out	High unit cost; limited “spare” vehicles		Multiple spare vehicles	Re-launch readily available
					<12 months



Sharing JPL COTS Radiation Guidelines. Not a Good Example

1 Guideline for the Selection of COTS Electronic Parts that will operate in a Space Radiation Environments 1-1

2 Radiation-Based Selection of COTS Devices for JPL Flight Systems: Field Programmable Gate Arrays (FPGA) 2-2

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technology nodes). The primary design tradeoff for using these devices is that they are volatile, requiring an external configuration memory to store the configuration data; this adds design overhead, real-estate, power and additional reliability concerns to the system.

2.2.2 Flash-based architecture

A flash-based FPGA architecture replaces SRAM configuration elements with floating gate flash technology. The primary benefit being the configuration is non-volatile, meaning it is live on power-up and does not require external memory. The flash process is typically more efficient in terms of area and power. One drawback to flash-based FPGA is that the number of erase-program cycles is limited, unlike SRAM. However, that number is typically in the 10,000 to 100,000 range, which is more than enough for most space applications. Another drawback is that it is a non-standard CMOS process, meaning it will lag behind the aggressively scaled SRAM architecture. Microsemi, formerly Actel Corporation, is the main manufacturer of flash-based FPGAs.

2.2.3 Antifuse-based architecture

Finally, antifuse-based FPGAs implement one-time-programmable (OTP) switches to route and define logic elements. The advantages to this technology are its non-volatility and very small area overhead. The clear disadvantage is the inability to reprogram functionality, and the non-standard CMOS process required to produce the FPGAs. Microsemi and Aeroflex are the two primary manufacturers of antifuse FPGAs.

2.3 RADIATION EFFECTS ON FPGA TECHNOLOGIES

This section provides an overview of radiation effects on the three main FPGA technologies. While not intended to be a comprehensive review of radiation effects, the goal is to provide enough information to aid in the selection of the right COTS FPGA technology for a particular JPL flight mission and/or application.

2.3.1 Destructive Effects – Single Event Latchup – Any FPGA Containing CMOS

2.3.1.1 Overview

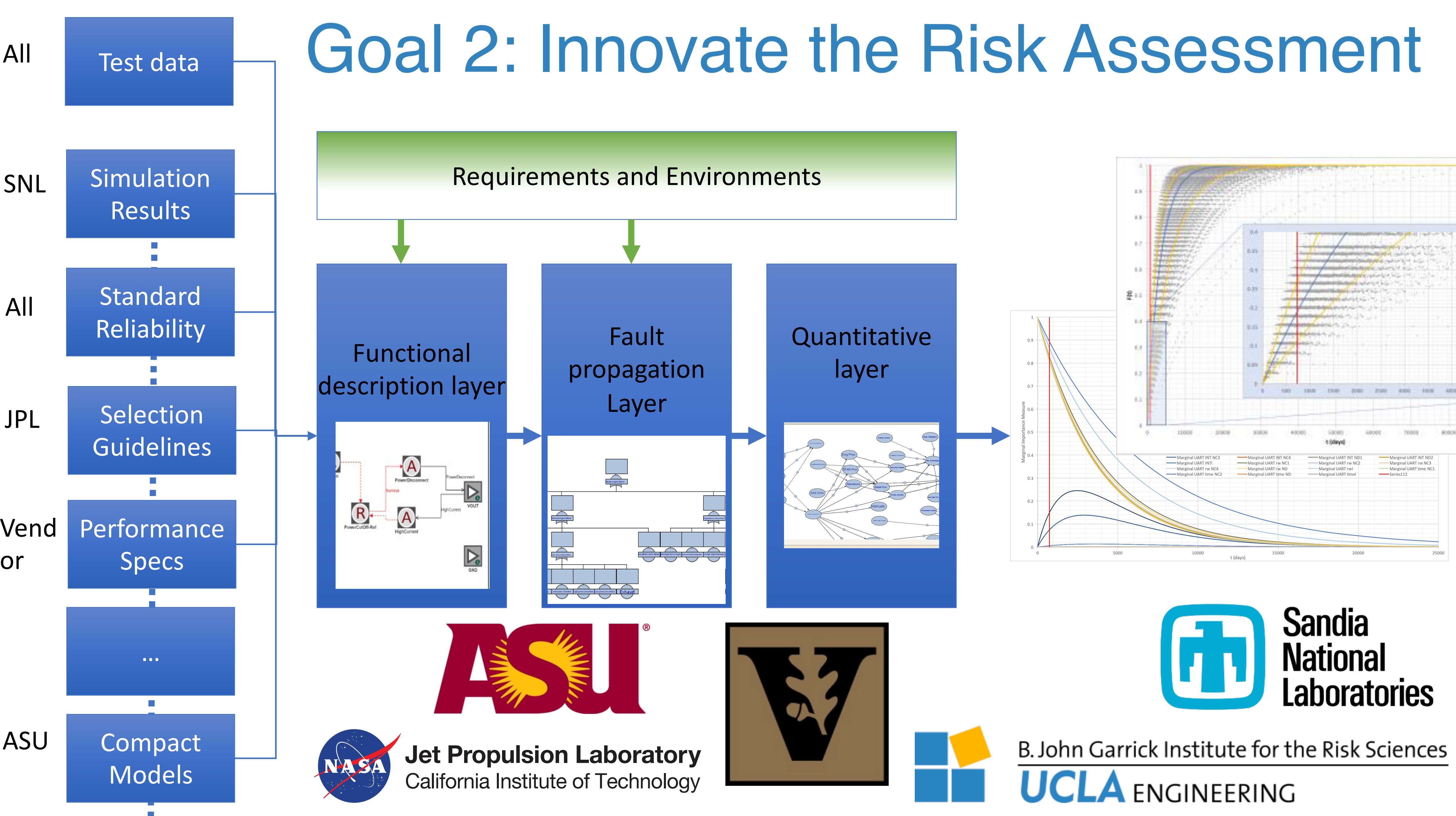
CMOS technology is potentially susceptible to single event latchup (SEL). SEL susceptibility in these devices can range from complete immunity, to very rare events, to extremely frequent and/or destructive events.

Basic Knowledge Sharing Made Easier

M-2 Microcircuits

Type	Overview/General Construction	Circuit Applications	Common Failure Modes	Failure Mechanisms	Technology Trends	Reliability	Recommendati
NVM, NOR Flash Single-level Cells	split-gate-based. Floating-gate-based and split-gate-based use a floating poly-Si gate to store the data while the charge-trapping type uses nitride (Si3N4) for charge storage. They all employ channel hot electron mechanism to program and tunneling for erase. Generally available in TSOP and BGA packages. • Stacked-gate Split-gate	its random access capability. Faster read and write compared to NAND Flash. Technology of choice for embedded applications.	* Data retention due to charge loss at higher temperature (>150°C) * Over-erase bit causing excessive bit line leakage * Degradation of charge pump efficiency * Gate oxide rupture	of trap sites and interface states inside oxide) from P/E cycling is the root cause of failures. * Stress induced leakage current (SILC) attributed to data retention failure	data retention compared to both floating-gate and charge-trapping types. However, its density (~64Mb) is relatively small as compared to floating-gate and charge-trapping (~1Gb). The major Floating gate vendors are Micron, Atmal and Intel. Split gate vendor: Microchips (formally SST) Charge Trapping (Mirror bit) Vendor: Cypress (formally Spansion)	quality of the tunnel oxide. They are sensitive to P/E cycle, extended read conditions.	PE cycles and operating temperature. easily degraded under excessive radia Recommend a derating factor of 0.75 rated endurance cycles from manufactu Use Hamming ECC at a minimum. Per cycling at min, max & nom. Vcc to fu over life for critical applications.
NVM, NOR Flash Multi-level Cells	Only the Floating-gate and Charge-trapping type offer MLC (two bits per cell), e.g., Intel's StrataFlash and Spansion's mirror-bit technologies. Intel's StrataFlash employs different charge density in the floating gate to store 2 bits of information. Spansion's mirror bit employs charge trapped near the source and drain junctions to store 2 bits max. of information.	Widely used for code storage due to its random access capability. Faster read and write as compared to NAND Flash. Technology of choice for embedded applications.	* Read window closure due to excessive P/E cycle. * Data retention failure due to charge loss at higher temperature (>150°C) * Over-erase bit * Over-program bit * Gate oxide rupture	* Electron trapping and charging attributed to cycling-induced failures. * Stress induced leakage current (SILC) attributed to data retention failure.	Currently not widely offered by the vendors. MLC is typically offered for NAND-based Flash.	MLC NOR is generally less reliable than SLC. Typically the endurance spec will show a 10x difference (10K for MLC, 100K for SLC).	MLC Flash is not recommended for u application. Extra consideration need ECC.
NVM, NAND Flash Single-level Cells	The basic storage cell in a mainstream NAND flash is similar to NOR. The key difference is how these storage cells are connected. For NAND, there are a total of 16 to 32 storage cells connected in series with two select transistors at the top and bottom of the string. NAND employs Fowler Nordheim tunneling mechanism for both program and erase. NAND SLC has a 2D planar topology compared to the more advanced 3D-NAND.	Widely used for data storage, e.g., thumb drive, solid date disk drive) due to its low bit cost (< $1 per Gb).	* Read window is widening due to excessive P/E cycles. * Charge loss leading data retention failure at high temperatures. * Degradation of charge pump efficiency under radioactive environment.	* Electron trapping and charging attributed to cycling-induced failures. * Stress induced leakage current (SILC) attributed to data retention failure. * High voltage operations resulting in severe cell-cell interference and program disturbs.	2D NAND encounters scaling challenges at 10 to 19 nm node. Vendors have gradually migrated towards 3D-NAND topology to continue with the NAND scaling.	NAND shares common reliability problems with NOR. Cycling-induced oxide degradation is one major issue.	SLC NAND is considered to be more MLC NAND. The endurance spec for typically rated up to 10K cycles. Rec factor of 0.75 for Vmax, Imax and rate from the manufacturer's data sheet. A chip is typically introduced for giga-b (>Gb) for efficient and reliable data ma garbage collection, bad blocks). Use Reed-Solomon ECC. Perform end min, max & nom. Vcc to fully charact critical applications.
NVM, NAND Flash Multi-level Cells	Multi-level cells in 2D-NAND still adopt the SLC NAND string structure. The key difference is how the cells are programmed to different levels. Three types of multi-level cells are available - MLC (2 bits/cell), TLC (3 bits/cell) and QLC (4	Widely used for data storage, e.g., thumb drive and solid state disk drive due to its low bit cost (< $1 per Gb).	* Read window widening due to excessive P/E cycles. * Charge loss leading to data retention failure at high temperate. * Degradation of charge pump efficiency under radiative environment.	* Electron trapping and charging attributed to cycling-induced failures. * Stress induced leakage current (SILC) attributed to data retention failure.	Transition of 2D-NAND towards 3D-NAND started in late 2016.	Reliability of MLC NAND is worse than its SLC counterpart. An obvious differentiator is the endurance specs: < 1K for MLC versus 10K for SLC.	MLC Flash is not recommended for u applications. Extra considerations ne

Appendix A | Capacitors | Diodes | Optoelectronics | Microcircuits | Resistors | Thermistors | Transistors | +


Goal 2: Innovate the Risk Assessment
All
Test data
SNL
Simulation Results
All
Standard Reliability
JPL
Selection Guidelines
Vendor
Performance Specs
...
ASU
Compact Models
Requirements and Environments
Functional description layer
Fault propagation Layer
Quantitative layer
ASU
Sandia National Laboratories
Jet Propulsion Laboratory
California Institute of Technology
NASA
B. John Garrick Institute for the Risk Sciences
UCLA ENGINEERING

Types of Information

- In ideal world we have on or all of:
  - Test Data (e.g., normal, accelerated)
  - Supplier test data
  - Supplier reliability estimates
  - Clear, solid instructions (i.e.
- Typically, we have incomplete data:
  - Test and Mission performance data on similar, but not identical, parts
  - Estimates based on POF modeling and simulation
  - Historical, on orbit, performance data
- Somewhat useful but hard quantify:
  - Expert Assessment
  - Adjustment Factors, Weights of Evidence
  - Qualitative Factors

Lessons learned at the system level (i.e. can I charge battery while tumbling)

1

Assumption:1
Radiation tests are performed on parts with the same part number and manufacurer but nothing is known about the lot.

Goal:2
System and its elements are designed to withstand nominal and extreme loads and stresses (radiation) for the life of the mission (NASA R&M).

Justification:1
Heavy-ion SEL tests were not performed because the heavy-ion environment does not significantly contribute to the radiation environment.

Or
ChoiceJn

Strategy:6
Process does not have parasitic thyristors.

Strategy:3
Perform proton SEL characterization tests on system parts.

Strategy:4
Perform TID characterization tests on system parts.

Strategy:5
Effects of SEL are mitigated on system parts.

Goal:5
COTS parts pass mission proton SEL requirement: No latch-up seen up to 5e9 (p/cm2) protons.

Goal:6
COTS parts pass TID requirement at 30 krads(SiO2).

Context:5
Parts that did not pass proton SEL requirement or did not have proton SEL testing performed: Microcontroller, WDT, regulators, logic translator, and mux/demux.

Goal:10
Current Monitor (INA193AIDBVR) passes SEL mission requirement.

Goal:19
Microcontroller (PIC24FJ256GB210-I/PT) passes TID mission requirement: Supply current <18mA, runs flight program, and can be reset.

Solution:3
Results from IUCF: No latch-up seen on Current Monitor up to 5e10 (p/cm2) protons.

2

F1: Count Number of Upsets in SRAM
F2: Communicate with SRAM
F3: Communicate with Spacecraft
F4: Recover from SEEs
F5: Power SRAM
F6: Read/Write to SRAM
F7: Detect and Recover from SELs
F8: Detect and Recover from SEFIs

3

4

System-level mitigation strategies unknown

<< Block >> Bus::VUC_Bus
I2C_Bus
Power

<< Block >> Power::REM_Power
3V_Bus
3V_uC
3V_sw...
1.8V
0.9V
Core
CoreV
CoreC
Flags
WDI
Latch...
Power...
CoreSt...

<< Block >> Control::REM_Control
3V_uC
I2C_Bus
CoreV
CoreC
Flags
WDI
Latch...
Power...
CoreSt...
Data
Address
Control

<< Block >> LogicTranslation::REM_LogicTranslation
3V_uC
3V_sw...
1.8V
Data
Address
Control
Addres...
Data_In
Data_...
Contro...

<< Block >> SRAM::28nm_SRAM
1.8V
0.9V
Core
Addres...
Data_in
Data_o...
Control

I2C_Bus
Core
0.9V
1.8V
3V
3V_Switch
1.8V
3V_uC
3V_uC
Core_Voltage
Core_Current
Flags
WDI
Latch_PowerStale
PowerStale
CoreStale
Data
Address
Control
Address_T
Data_in
Data_out
Control_T

5

Single Event Environment

SEU
Absent 50%
Present 50%

Vdd
Correct 100%
Low 0%

Input
Correct 100%
Incorrect 0%

Data
Clean 80%
Corrupted 20%

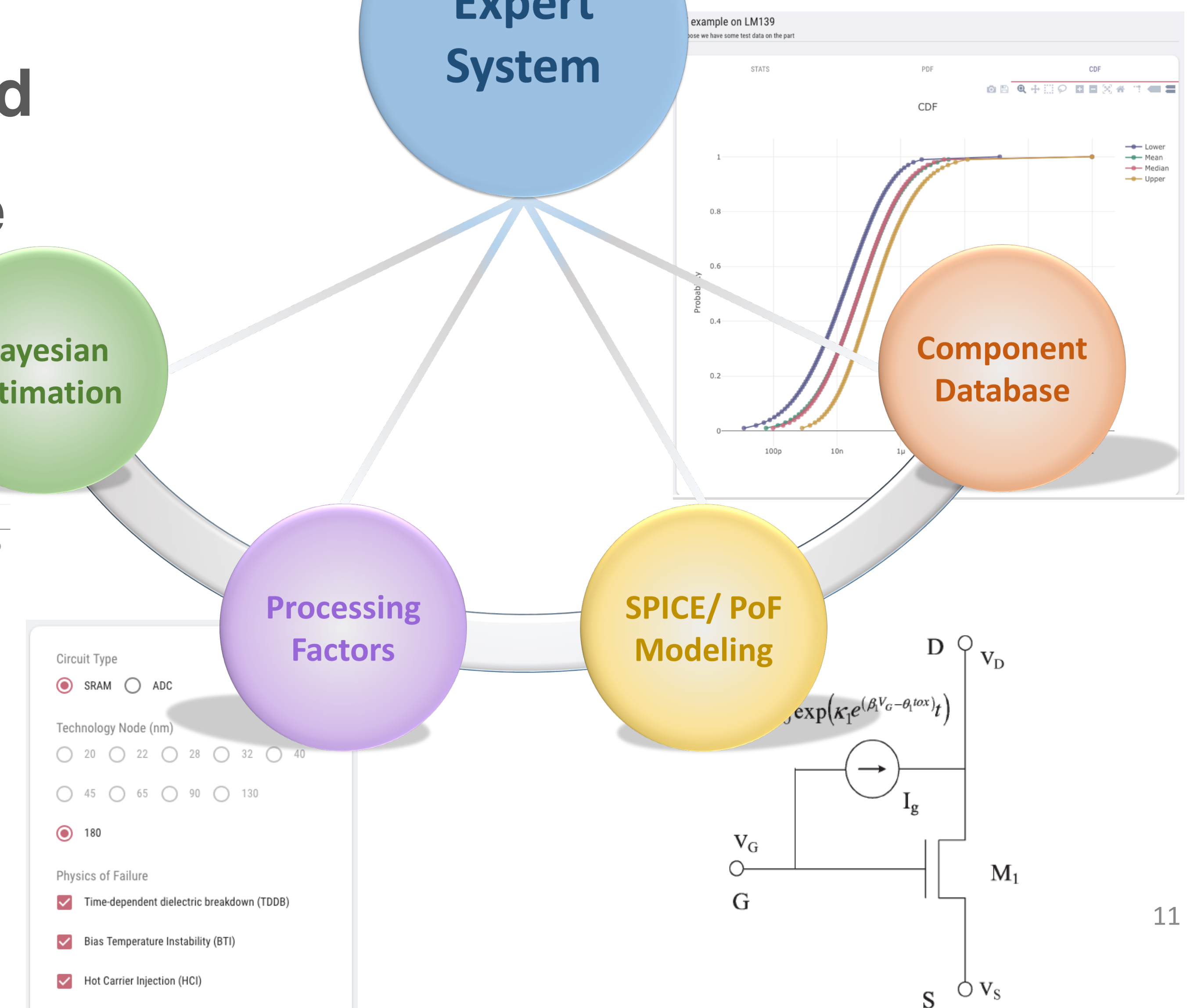
Word
Correct 100%
Wrong 0%

SRAMData
Good 84%
Bad 16%

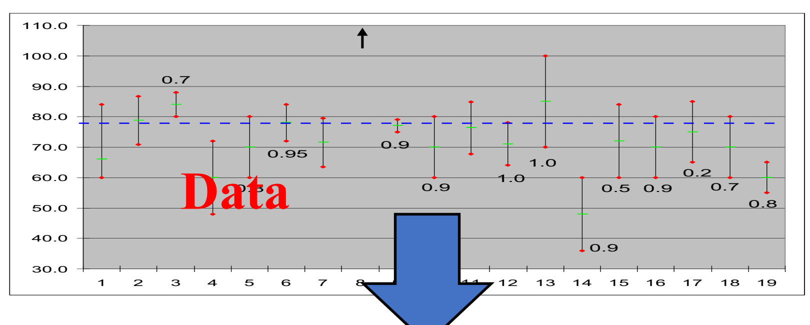
A Predictive Tool

UCLA

The Expert System is a guided tool that gives the analyst the capability of aggregating various reliability related evidence about a COTS part to obtain an estimate for its failure rate.

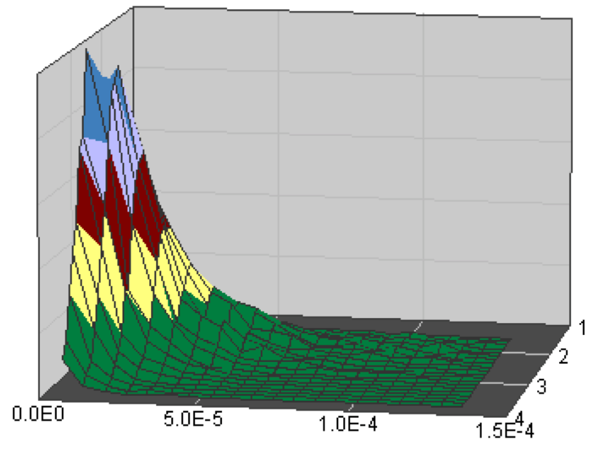


Aggregation of Multiple Pieces of Information

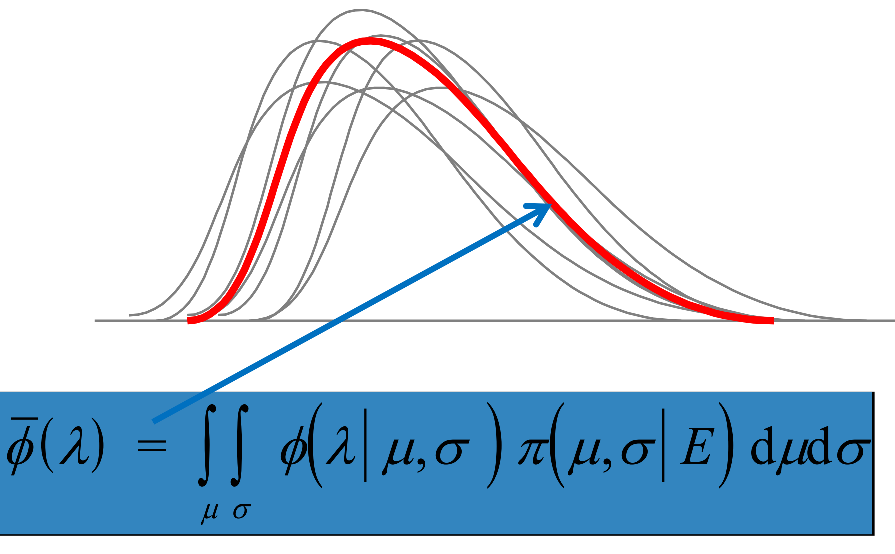


$$\pi(\mu,\ \sigma \mid E) = \frac{\mathrm{L}(E \mid \mu,\ \sigma)\ \pi_o(\mu,\ \sigma)}{\int_\mu \int_\sigma \mathrm{L}(E \mid \mu,\ \sigma)\ \pi_o(\mu,\ \sigma)\ \mathrm{d}\mu\, \mathrm{d}\sigma}$$

$$E = \{k_i,\ \mathrm{T_i}\}\ \mathrm{i} = 1,\ \ldots,\ \mathrm{N}$$



Bayes Theorem



$$\bar{\phi}(\lambda) = \int_\mu \int_\sigma \phi(\lambda \mid \mu,\sigma)\ \pi(\mu,\sigma \mid E)\ \mathrm{d}\mu \mathrm{d}\sigma$$

COTS Electronic Parts Reliability Assessment Expert System

Circuit Simulation at a Glance

Circuit Type

SRAM ADC

Technology Node (nm)

20 22 28 32 40

45 65 90 130

180

Physics of Failure

Time-dependent dielectric breakdown (TDDB)

Bias Temperature Instability (BTI)

Hot Carrier Injection (HCI)

Mission Time (hours)

27778 hrs

Temperature (˚C)

27 ˚C

SAVE RUN

ADC Failure Criteria

Effective Number of Bits

Offset Voltage
Import Offset Voltage (mV) from Cadence — OFFSET VOLTAGE

Threshold Resolution
Threshold Resolution (bits) — Resolution Threshold 6 bits

Ideal Resolution
Ideal Resolution (bits) — Ideal Resolution 10 bits

Operating Voltage
Operating Voltage (V) — Operating Voltage 1.8 V

ENoB Before Degradation
Effective Number of Bits Before Degradation — ENoB Before Degradation 10 bits

SAVE

SRAM Failure Criteria

Bit Error Rate Standby Power Increase

Cell Power Increase
Cell Power Increase from Cadence — Cell Power Increase 100

Power Increase
Standby Power Increase Criterion — Power Increase Criterion 0.1

SRAM Size
SRAM Size (bits) — SRAM Size 1024 bits

SAVE

SRAM Failure Criteria

Bit Error Rate Standby Power Increase

Intrinsic SNM
Upload intrinsic static noise margin data (Optional) — INTRINSIC

Degraded SNM
Upload degraded static noise margin data from Cadence — DEGRADED

SAVE

Circuit Simulation – Flowchart

COTS part

Database search:
1. In: COTS parts name
2. Out: COTS parts data sheet. (Info. of COTS)

Technology node Database:
1. In: COTS part data sheet
2. Out: manufacturer information and technology physical parameters.

Operating condition

Physic of Failure Models:
1. In: trx. parameters for failure calculation.
2. In: Op. conditions for failure calculation.
3. Out: Probability that PoFs occur.
4. Out: trx. chars degradation over time.
5. Out: Equivalent ckt. elements that reflect the degraded chars. (for SPICE).

Failure time

PDKs

Circuit information:
1. In: COTS part data sheet
2. Out: Circuit type (for SPICE)
3. Out: canonical cell (for SPICE)
4. Out: performance metrices (for failure criteria)

User-defined Criteria

PoFs equivalent ckt. elements

SPICE Simulation:
1. In: tech. PDKs, PoF equivalent ckt, ckt Config.
2. Out: cell performance w/ degradation.
3. Out: The time that the cell hits the failure criteria.

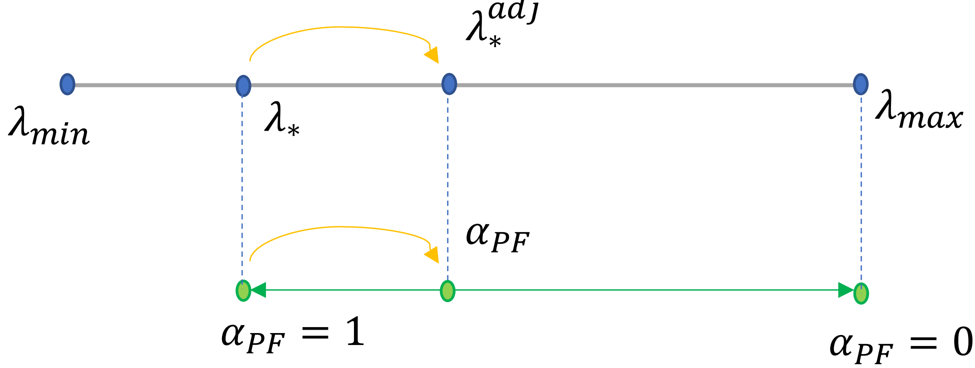
Determine the failure:
1. In: cell performance (SPICE)
2. Out: cell failure estimation

Ckt. Config.

canonical cell failure criteria

Process Factors

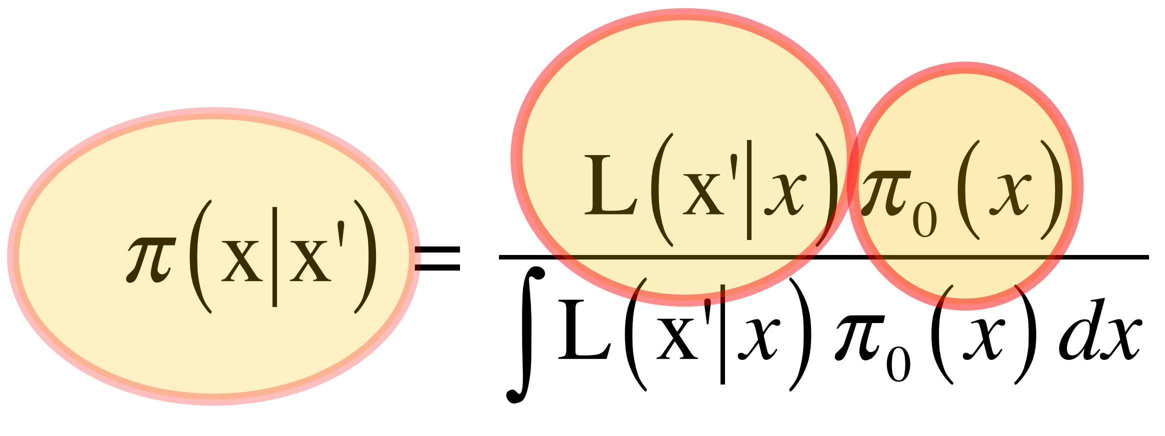
- **Bayesian Network is used to integrate the effect of all these factors on reliability estimation**
- **The result is a process factor coefficient $0 \leq \alpha_{PF} \leq 1$ which reflects the credibility of the manufacturer**



Reputation
Push design rules
Trust Relationship
Margining
Multiple Fabs
Following Reli. rules
Design
Maturity
Defectivity metrics
Teardown
Publish Process details
SPC
Process
Reliability Guideline
Manufacturer Credibility Factor
WAC
Grade
Fab
Volume
Size
Burn-in
Redundancy
Product
BB Screen
Spec.Sheet
HV. OEM

Backup

Addressing the Challenge through Bayesian Framework



$$\pi(\mathrm{x}|\mathrm{x}') = \frac{\mathrm{L}(\mathrm{x}'|x)\,\pi_0(x)}{\int \mathrm{L}(\mathrm{x}'|x)\,\pi_0(x)\,dx}$$

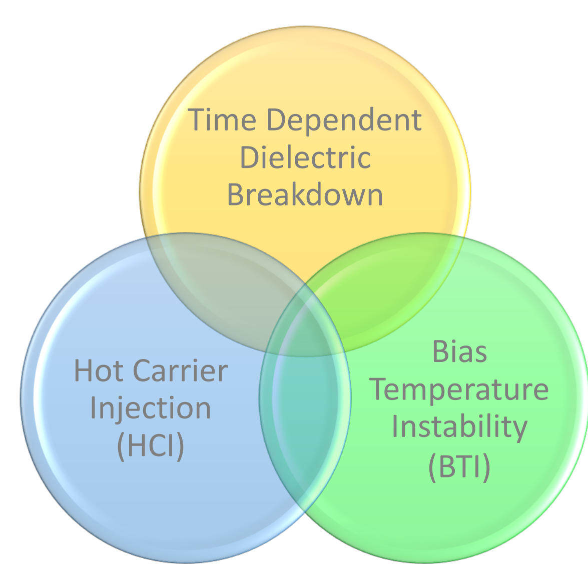
Prior PDF
Posterior PDF
PDF
0.6
0.5
0.4
0.3
0.2
0.1
0
0.001
0.01
0.1
1
10
100
1000
X

X = Unknown to be estimated

X' = Evidence

Circuit Simulation with Physics of Failure

- **Considers the Circuit Simulation with Physics of Failure (PoF)**
- **Three stages:**
  - **Stage I - Preprocessing:**
    - Modeling the Physics of Failure of Transistors
    - Extracting physical properties required for circuit simulation
  - **Stage II - Simulation:**
    - Identifying the canonical block
    - Performing Circuit Simulation with Cadence
  - **Stage III - Post-Processing:**
    - Translating the results of Circuit Simulation to reliability metrics (i.e., Failures-in-Time)

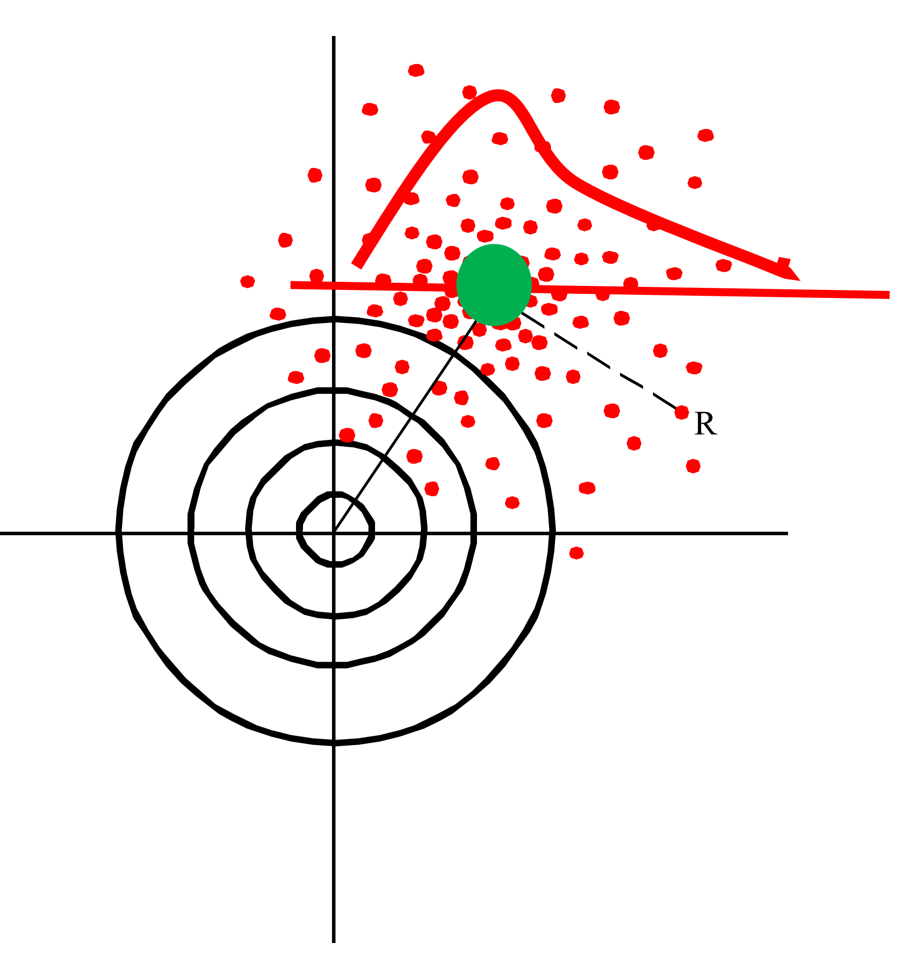


Modeling the Evidence – An Example

Additive Error Model:

$$x^* = x + E$$

$$L(x_1^*|x) = \frac{1}{\sqrt{2\pi}\sigma_1} \exp\left(-\frac{1}{2}\left(\frac{x_1^* - (x + b_1)}{\sigma_1}\right)^2\right)$$



COTS Electronic Parts Reliability Assessment Expert System

At a Glance

Component Select One	NEW	ALM2402QDRRRQ1	EDIT	0.10	FIT
Bayesian Estimation Model Select One	NEW	Homogeneous (LN, Percentile) (LN, Median_EF)	EDIT	6.40	FIT
Circuit Simulation Model Select One	NEW	SRAM 180nm CS	EDIT	0.0026	FIT
Process Factor Model Select One	NEW	SRAM 180nm PF	EDIT	0.881	

SAVE   Aggregated 1.194 FIT   ESTIMATE

Leveraging Expert Knowledge

- **Domain knowledge**: knowledge of the expert relative to the problem at hand
- **Normative expertise**: experts' ability to express domain knowledge in the form of metrics of interest

Bayesian Estimation of Data

The 12% increase in weighted average MME via Median aggregation, between s=2 and s=3 is due to the possible permutations of samples from a single SeqID with four e' observations, two of which have large MMEs > 400,000. Without this SeqID, the average MME would drop by 93%.

For both methods of aggregation, there is an order of magnitude reduction in average MME between s=1 and s=2; and between s=2 and s=4. A further factor of two reduction occurs between s=4 and s=5; and a factor of seven improvement between s=5 and s=7. After that, improvement essentially stops: results for s=7 through s=12 fall within (0.81a, 1.07a), where a denotes the average MME over this range of s.

Weighted Average MME—Probabilistic Data

1000
100
10

1 2 3 4 5 6 7 8 9 10 11 12

Number of Heads, s

MME via Median
MME via geomean

Part Reliability Database

- **Library of reliability data of electronic parts**
- **Rich source to infer the failure rate of parts and adjust it for specific application temperature**
- **Connectivity to open data bases (e.g., Texas Instrument database)**

Query Tool

Im

Manufacturer Part Number	Manufacturer
ALM2402FQPWPRQ1	Texas Instruments
ALM2402QDRRRQ1	Texas Instruments
ALM2402QPWPRQ1	Texas Instruments
CF99700AGLMM	Texas Instruments
CF99701GLMM	Texas Instruments

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Parts Database

Details				MTBF Rate							Early Life Failure Rate			
Part Name	Part Type	FIT	Activation E...	Fails	MTBF	Test Temp (C)	Confidence ...	Usage Temp...	Sample Size	Test Duratio...	Fails	DPPM	Test Temp (C)	Con
ALM2402QD...	Capacitor (A...	0.1	0.7	0	10000000000	125	60	55	159230	1000	0	6	125	60
LM139 MD8	Microcircuit ...	2.6	0.7	0	378000000	125	60	55	4412	1000	0	20	125	60

Previous Page 1 of 1 5 rows Next

Circuit Simulation – Case Studies

- **Two of the most commonly used COTS parts are thoroughly studied**
  - **SRAM**
  - **ADC**

- **Failure criteria:**
  - **SRAM:**
    - Bit Error Rate
    - Standby Power Increase
  - **ADC:**
    - Effective Number of Bits

Effect of Manufacturing Process Factors

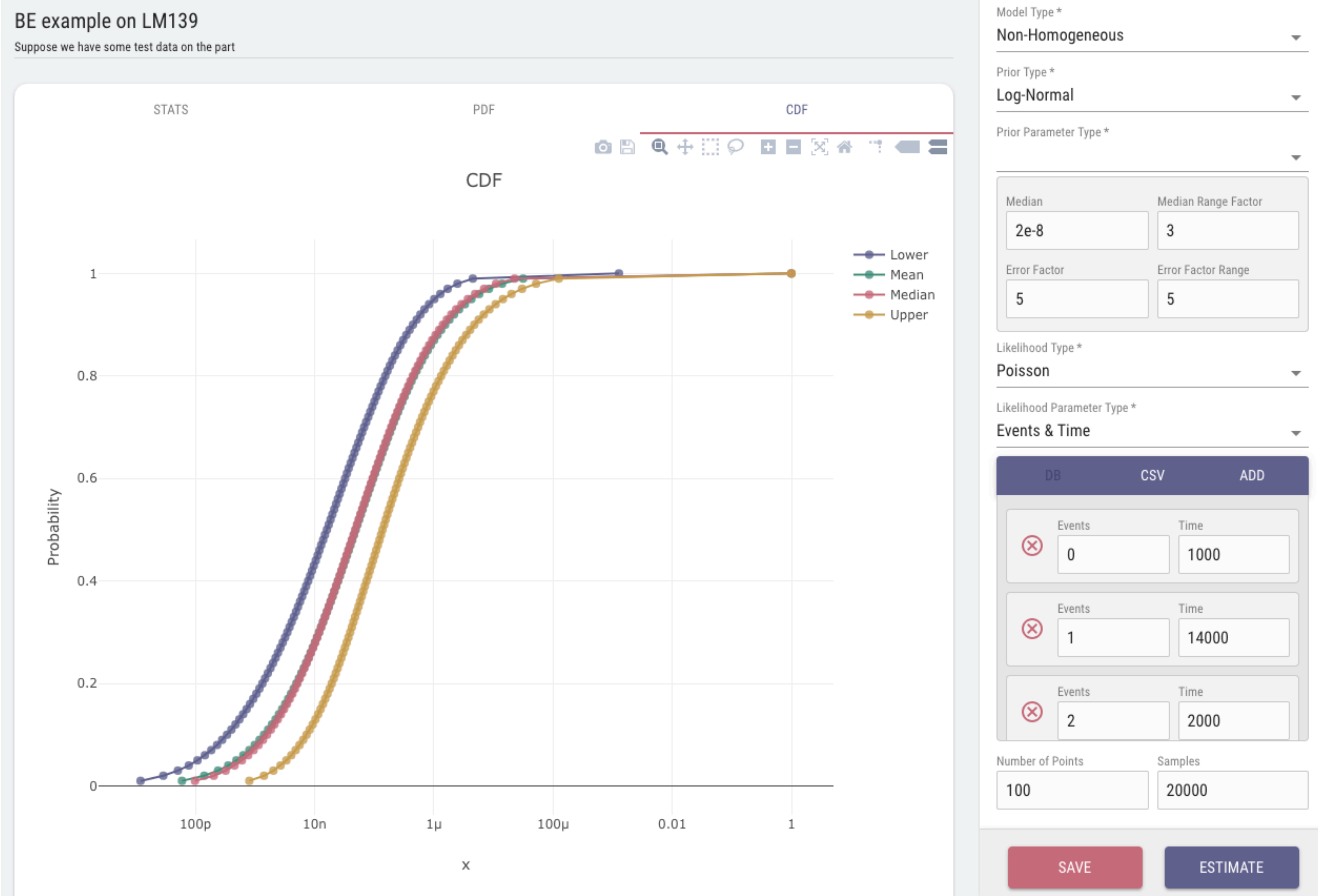
- **Qualitative manufacturing process factors that can affect the reliability of the parts**
- **Can be used to adjust an existing failure rate estimate**
- **These factors are characteristics of the manufacturing process**
- **Identified major factors by domain experts:**
  - **Fabrication related factors (Fab)**
  - **Design related factors (Design)**
  - **Process related factors (Process)**
  - **Product related factors (Product)**

Bayesian Estimation Module

- **Tool to integrate different pieces of information.**
- **Two types of analysis:**
  - **Homogeneous Sources of Information :**
    - **Assumes that the population from which the evidence is obtained is homogeneous, or alternatively, that the observations refer to the same system or group of systems that have the same reliability characteristics.**
  - **Non-Homogeneous Sources of Information:**
    - **Assumes that available data are from systems or components submitted to different operational and environmental conditions, design or production differences, and therefore present different reliability measures, such as different failure rates or probabilities of failure on demand.**

COTS Electronic Parts Reliability Assessment Expert System

Bayesian Estimation Module at a Glance



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Integration

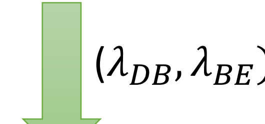
- **Expert System can handle the following use cases:**

Use case 1
- ● Part Database
- ○ Bayesian Estimation
- ○ Circuit Simulation
- ○ Process Factor

λ_{DB}

ES can quickly adjust it for Mission time and Operating temperature

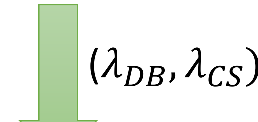
Use case 2
- ● Part Database
- ● Bayesian Estimation
- ○ Circuit Simulation
- ○ Process Factor



ES performs:
Non-Homogenous

Prior: λ_{DB}
Likelihood: λ_{BE} test data/ expert opinion

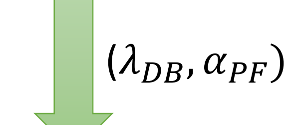
Use case 3
- ● Part Database
- ○ Bayesian Estimation
- ● Circuit Simulation
- ○ Process Factor



ES performs:
Non-Homogenous

Prior: λ_{DB}
Likelihood: results of CS (λ_{CS})

Use case 4
- ● Part Database
- ○ Bayesian Estimation
- ○ Circuit Simulation
- ● Process Factor



ES performs:
Linear α_{PF} adjustment

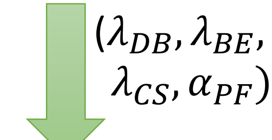
λ_{DB} will be adjusted based on information on manufacturer

Use case 5
- ● Part Database
- ● Bayesian Estimation
- ● Circuit Simulation
- ○ Process Factor

ES performs:
Non-Homogenous

Prior: λ_{DB}
Likelihood: Results of BE (λ_{BE}) and Results of CS (λ_{CS})

Use case 6
- ● Part Database
- ● Bayesian Estimation
- ● Circuit Simulation
- ● Process Factor



ES performs:
Non-Homogenous and Linear α_{PF} adjustment

Prior: λ_{DB}
Likelihood: Results of BE (λ_{BE}) and CS (λ_{CS})
The final result will be adjusted by (α_{PF})

COTS Electronic Parts Reliability

Expert System in HCLA

Parts Database

Circuit Simulation

Bayesian Estimation

Process Factor

System Engineering and Assurance

Expert System

Hybrid Causal Logic

Analysis Model

Supportive Model

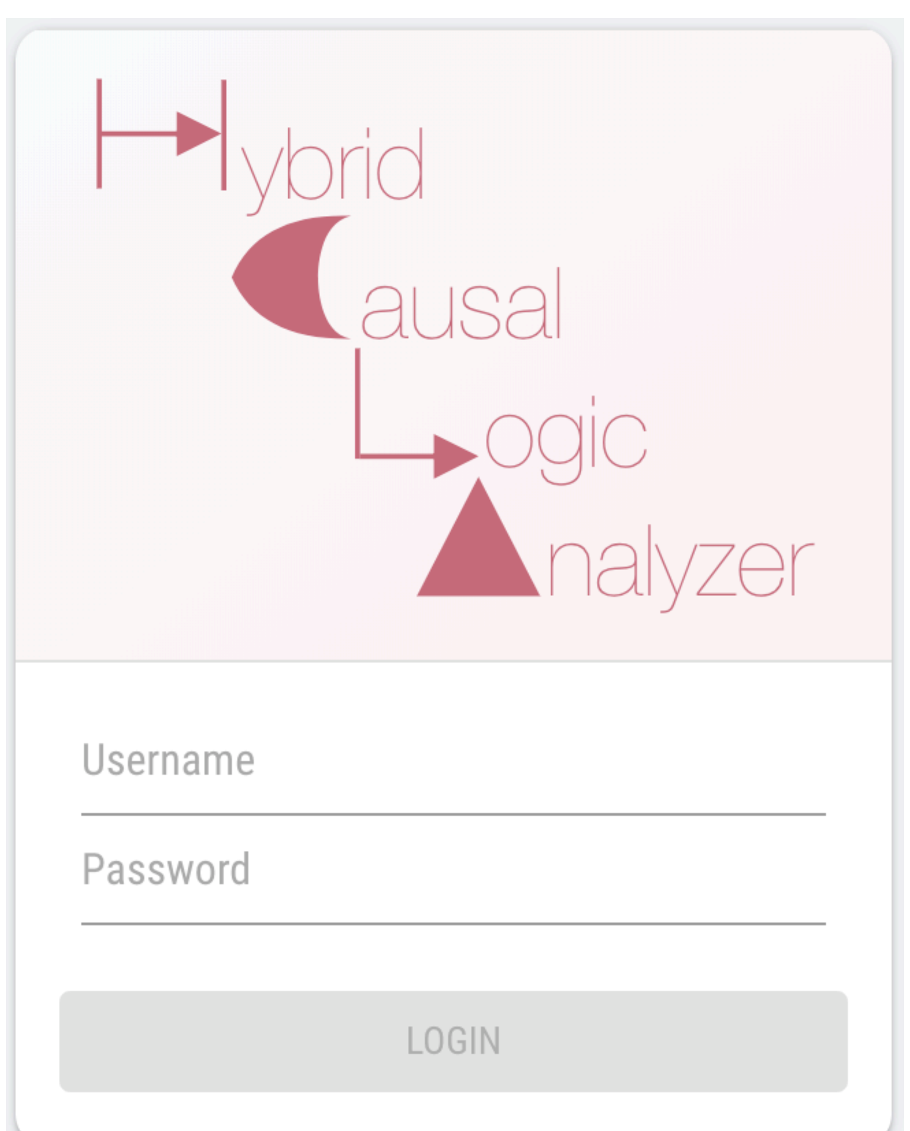
Model

Subsystem

Project

HCLA Demo

UCLA



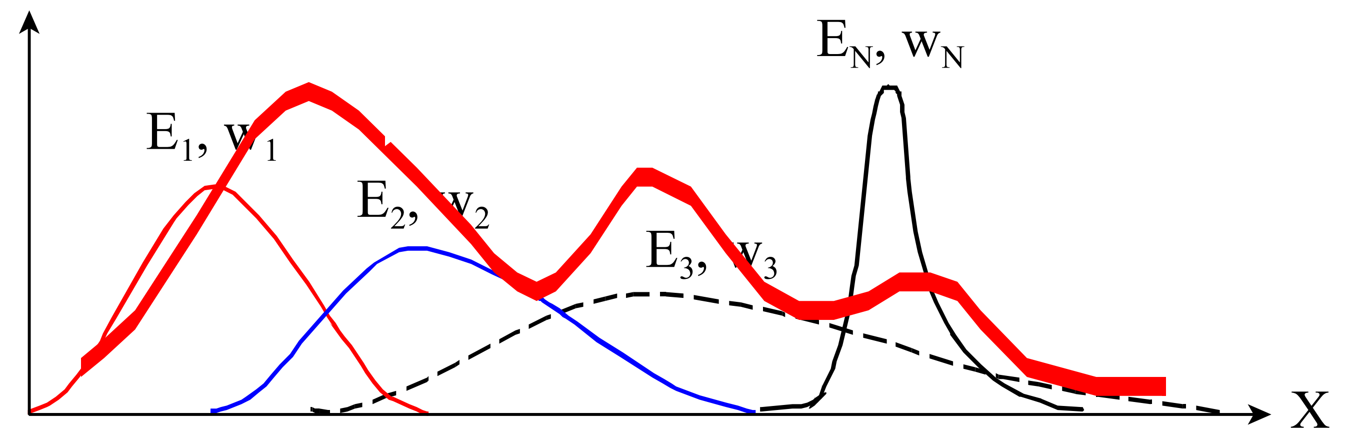
Backup

Bayesian Weighted Posterior Method

- Uncertain evidence: $E = \{E_i , w_i\}$ $i = 1, 2, \ldots, N$

$$\pi(x|E_i) = \frac{L(E_i|x)\,\pi_0(x)}{\int L(E_i|x)\,\pi_0(x)\,dx}$$

$$\pi(x|E) = \sum_{i=1}^{N} w_i\,\pi(x|E_i)$$



Constructing PoF equivalent circuit model

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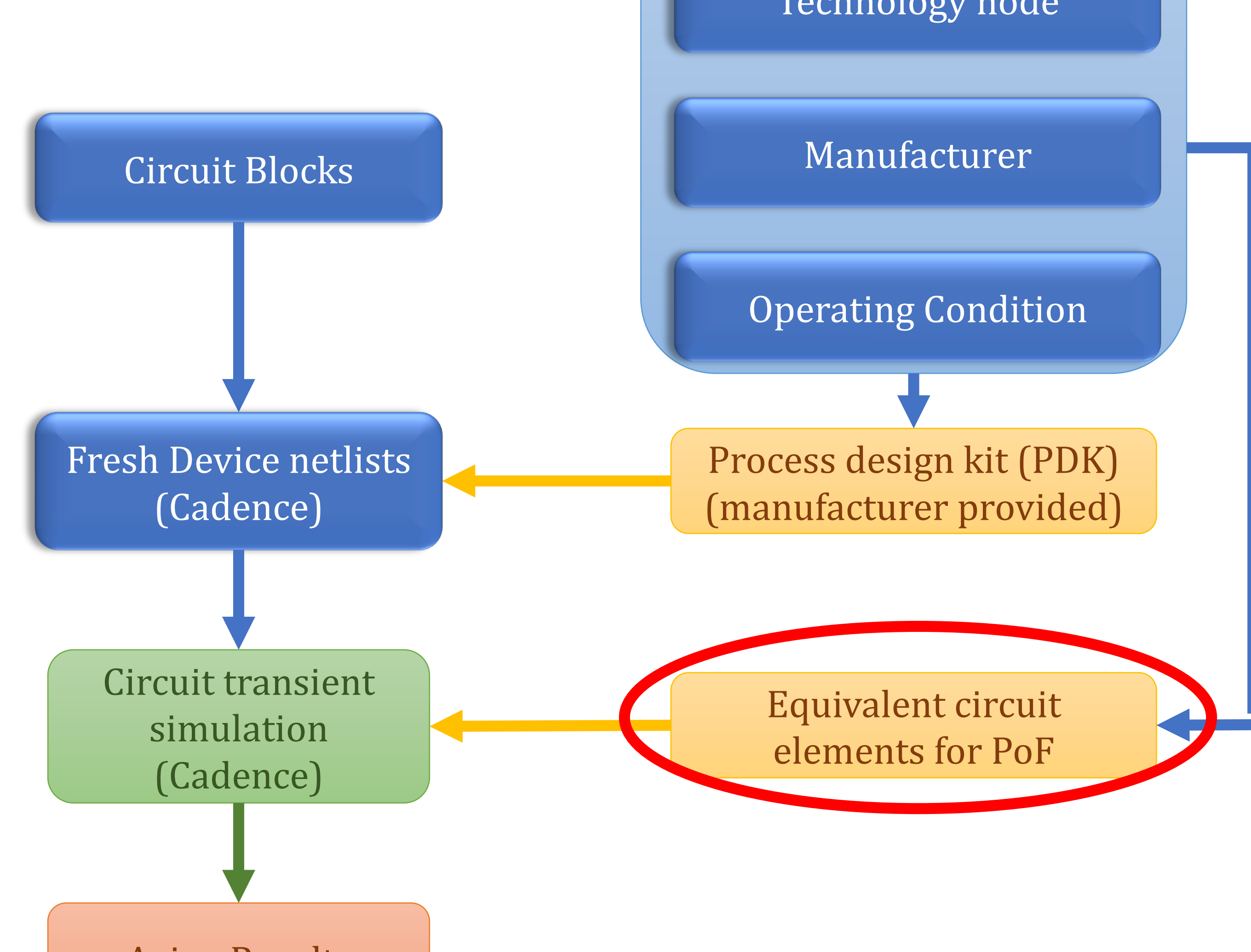
- Every Physics of Failure will be modeled as a set of equations.
- The Physics of Failure model can predict the device characteristic shifts over time.
- For every Physics of Failure, a equivalent circuit model will be developed for circuit simulation.



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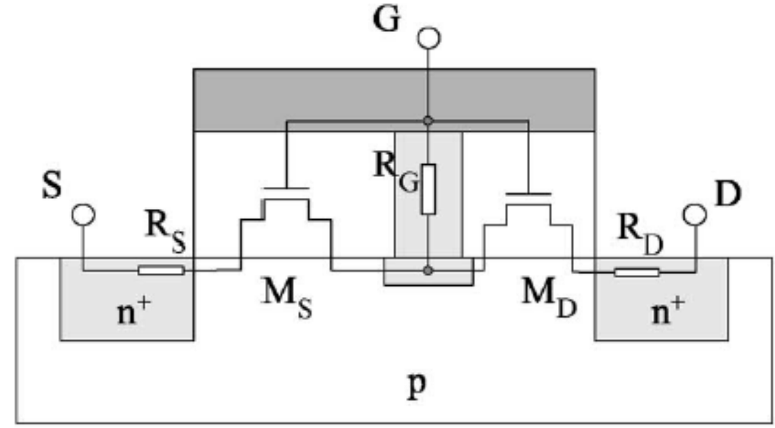
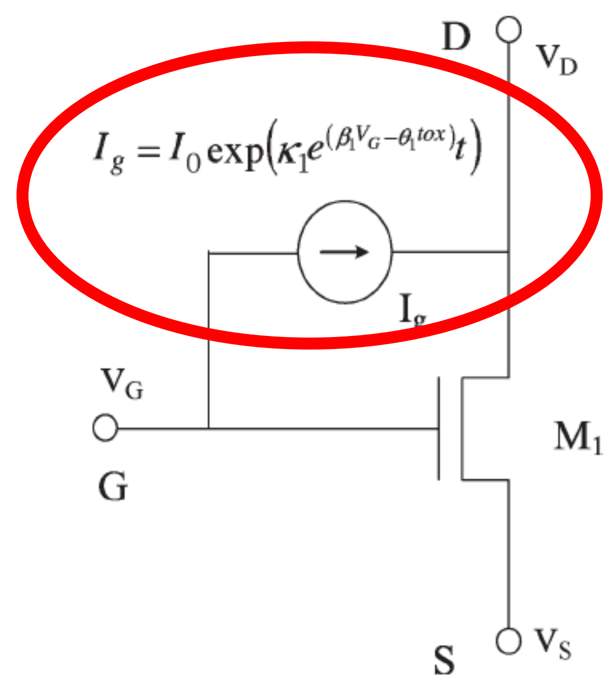
PoF Equivalent Circuit Model (TDDB)

- **Hard breakdown (HBD) model**
- **Instant increase in gate current**



- **Adding a Rg when HBD occurs.**
- **HBD follows Weibull distribution.**

- **Soft breakdown (SBD) model**
- **Gradual increase in gate current**

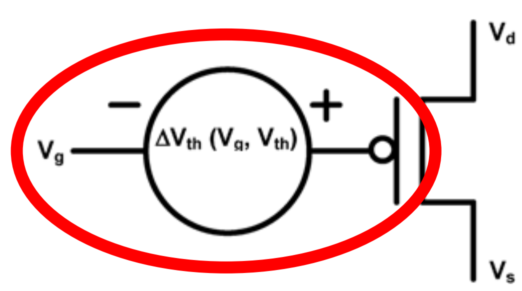


- **Gate current increase exponentially over time.**

$$I_g = I_0 \times \exp\left[\kappa_1 \times \exp(\beta_1 \times V_G - \theta_1 \times t_{ox}) \times t\right]$$

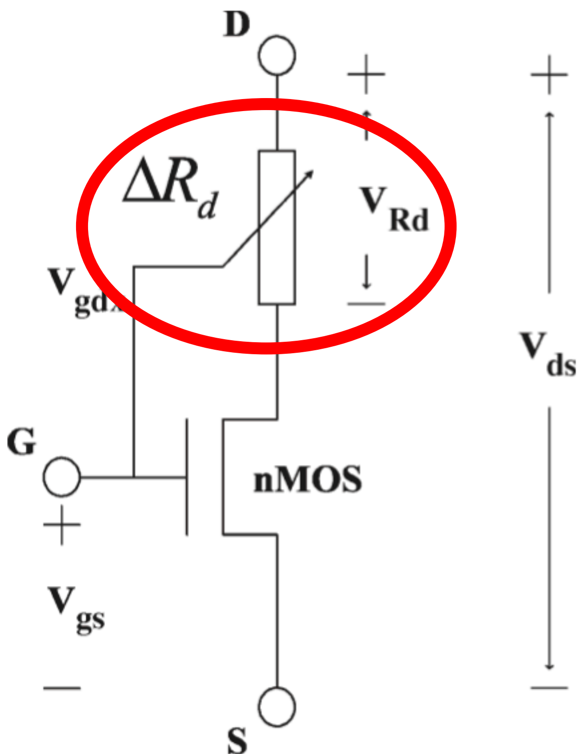
PoF Equivalent Circuit Model (N/PBTI)

- **BTI mainly impact threshold voltage shifts of a MOSFET transistor.**



$$\Delta V_{\mathrm{TH}} \approx A_0 \exp\left(-\frac{E_A}{k_B T}\right)\left(\frac{|V_G - V_{\mathrm{TH0}}|}{t_{\mathrm{ox}}}\right)^{\gamma} t_{\mathrm{stress}}^{n}.$$

PoF Equivalent Circuit Model (HCI)



$$V_{Rd} = -V_{gdx} + \sqrt{V_{gdx}^2 + 2V_{ds}\Delta N[\frac{\alpha\left(V_{gdx} + \frac{V_{ds}}{2}\right)}{1 + \alpha\Delta N} + \frac{q}{C_{ox}}]}$$

$$\Delta R_d = \frac{1 + \alpha\Delta N}{I_{ds0}} V_{Rd}$$

$$V_{gdx} = V_{gs} - V_t - V_{ds}\ (linear\ region)$$

$$V_{gdx} = 0\ (saturation\ region)$$

Assumption:

- **all interface traps are acceptor-like and occupied by elections**
- **Channel-mobility degradation u is caused by both** ΔN_{it} **and** ΔN_{ox}

COTS Electronic Parts Reliability Assessment Expert System

SRAM Degradation Modeling

Column Drivers

n-bit word

Bitcell Array

Bitlines for bit n

Address Decoder

Sense Amplifiers

Probability

Degradation

Failed

Noise margin

Assumptions:

- Gaussian distribution
- Variance remains
- Mean degradation
- Criterion: NM ≤ 0

Probability

Degradation

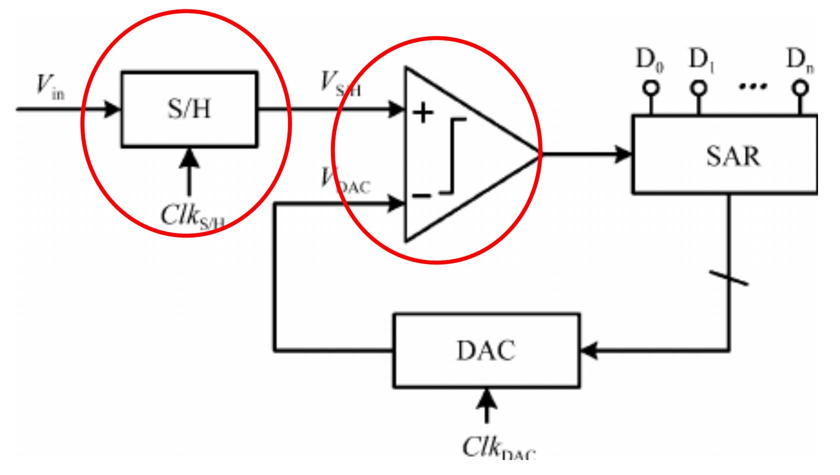
Failed

Power increase

Assumptions:

- Identical cell
- Binomial distribution
- Criterion: PI ≥ *x* %

ADC Degradation Modeling



Assumptions:

- S/H and comparators are critical
- Errors do not cancel (worst case)
- Criterion: ENoB
- Resolution is modeled by offset voltage change.