Independent Test Capability

Space Hardware

http://www.nasa.gov/centers/ivv/JSTAR/ITC.html

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NASA ITC
Independent Test Capability

Agenda

- **The Need for Space Hardware**
- **JSTAR Resources**
- **Use Case**

The Need for Space Hardware

Software Capabilities

- Software Models of Hardware have tremendous benefits:
  - Functionally equivalent
  - Portable/Sharable
- But still possess a few limitations:
  - Timing
  - Performance
  - Accuracy under Anomaly and Exceptions.

Timing

- Timing bugs can be some of the most difficult to resolve
  - May take hours/days to reproduce
  - Inconsistent
  - Often the result of complex interactions between multiple threads

Timing

- A Software Model is limited because it must model multiple chipsets in a single CPU

Simulation CPU

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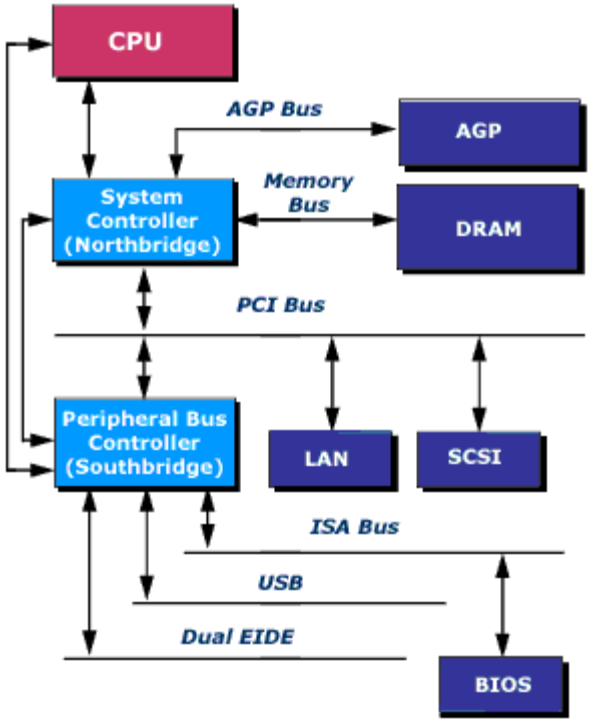
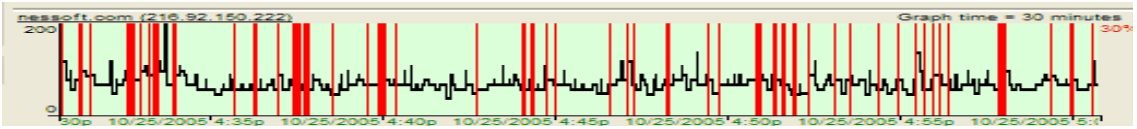


Timing

- Each chipset must be given *scheduled* CPU time in the host processor.
  - Asynchronous events (e.g. interrupts):
    - Only generated when chip is scheduled
    - Possibly arrive in a different order from hardware.
  - Latency/Jitter
    - Difficult to recreate exact timings between components. Software Model is virtually instant.



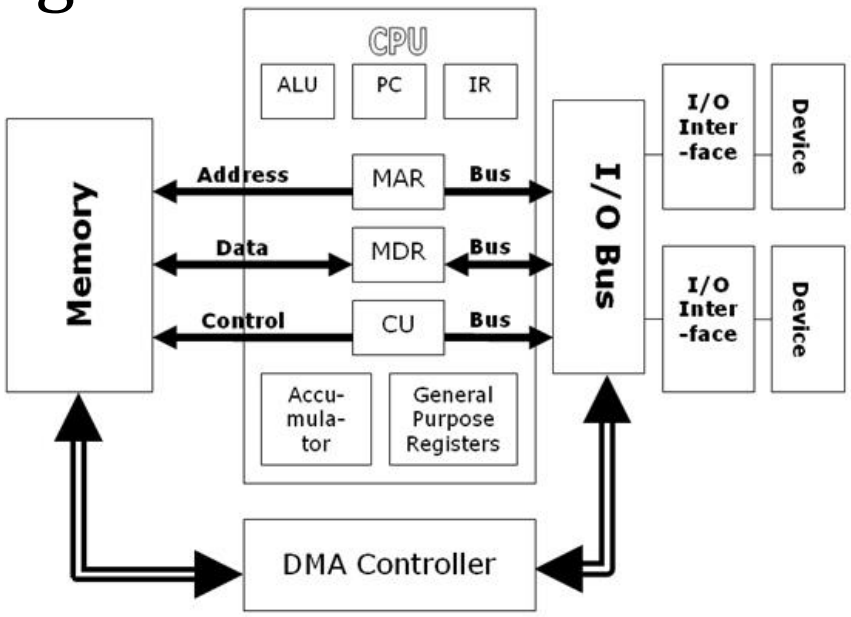
Performance

- The assembly instructions of each virtual chipset must be run by the host CPU for each chip in a virtual emulation.
  - This can make real-time difficult to achieve
  - Only matters if external components are interfaced
    - Ground Station
    - Dynamics Model
    - Hardware

Function	Address	Instruction
__ghs_eofn_init__7Exe...	0x00017050	addi r12,r12,6084
__ghs_eofn_init__7Exe...	0x00017054	stw r12,12(r3)
__ghs_eofn_init__7Exe...	0x00017058	li r11,0
__ghs_eofn_init__7Exe...	0x0001705c	stw r11,-32728(r13)
__ghs_eofn_init__7Exe...	0x00017060	beqlr
__ghs_eofn_init__7Exe...	0x00017064	b 0x1ce04
__ct__7ExecCSCFP11Exe...	0x00017068	stwu r1,-32(r1)
__ct__7ExecCSCFP11Exe...	0x0001706c	stmw r27,12(r1)
__ct__7ExecCSCFP11Exe...	0x00017070	mr r27,r8
__ct__7ExecCSCFP11Exe...	0x00017074	li r9,0
__ct__7ExecCSCFP11Exe...	0x00017078	mflr r0
__ct__7ExecCSCFP11Exe...	0x0001707c	stw r0,36(r1)
__ct__7ExecCSCFP11Exe...	0x00017080	mr r31,r3
__ct__7ExecCSCFP11Exe...	0x00017084	stw r9,0(r31)

Accuracy

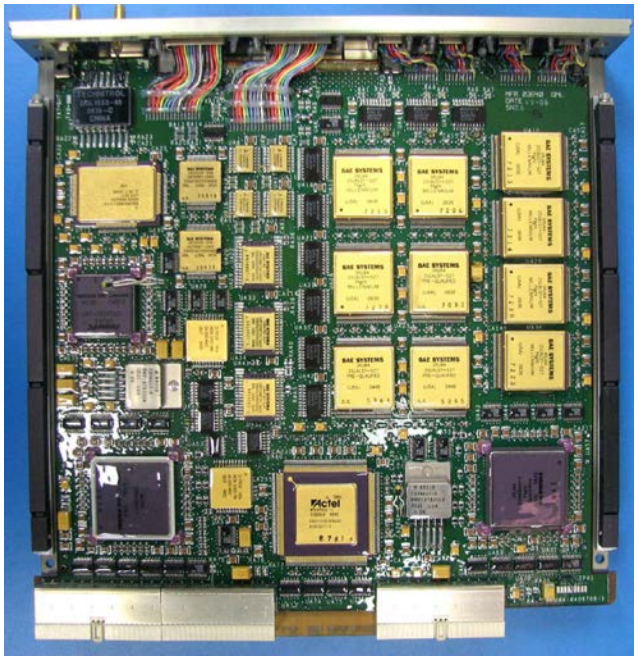
- Modelling hardware in software can be a tremendous undertaking
- It involves capturing:
  - Interrupts
  - DMA
  - Registers
  - Memory Maps
  - Buses (PCI, VME, etc)
  - Exceptions
  - Interactions of multiple components
  - Recreating system timings



Accuracy

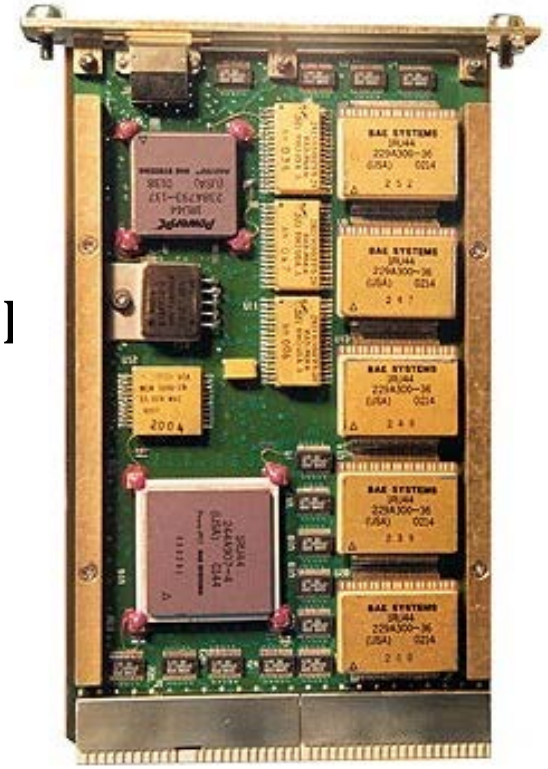
- Some of the problems that often occur when modeling hardware:
  - The hardware specification is not accurate nor complete
  - Due to the complexity of the task, often the nominal paths are modeled, but the exceptions and anomalies get left out.
  - Analog interfaces are free of noise
- In specialized cases, this can make recreating errors impossible.

JSTAR Resources



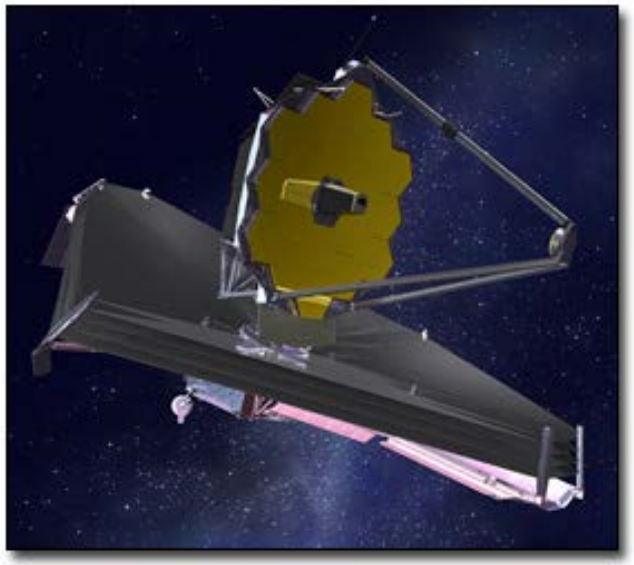
RAD750

- 2 Models:
  - 3U
    - 128 Mb RAM
    - 1553, SpaceWire, Ethernet on cPCI backplane
  - 6U
    - 36 Mb RAM
    - Integrated 1553 and SpaceWire



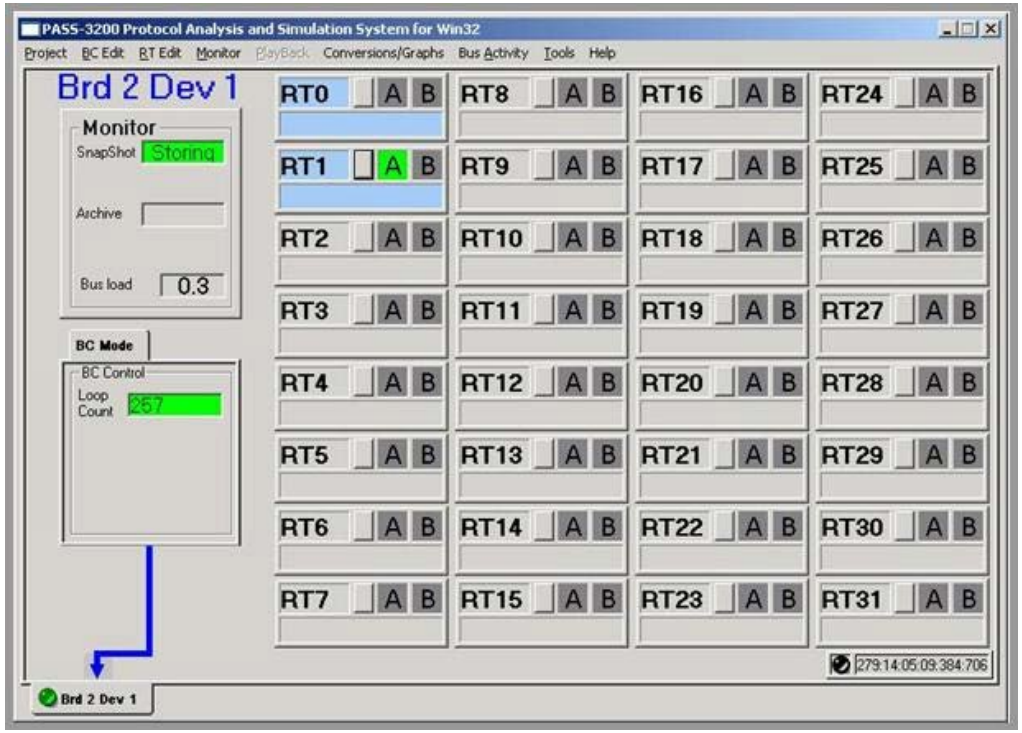
Mission Support

- The RAD750 is the de-facto processor for many NASA missions, including:
  - Deep Impact
  - Mars Reconnaissance Orbiter
  - STEREO
  - LRO
  - SDO
  - JUNO
  - GPM
  - JWST



Other Resources

- ITC has a variety of 1553 and SpaceWire test sets to simulate common space protocols

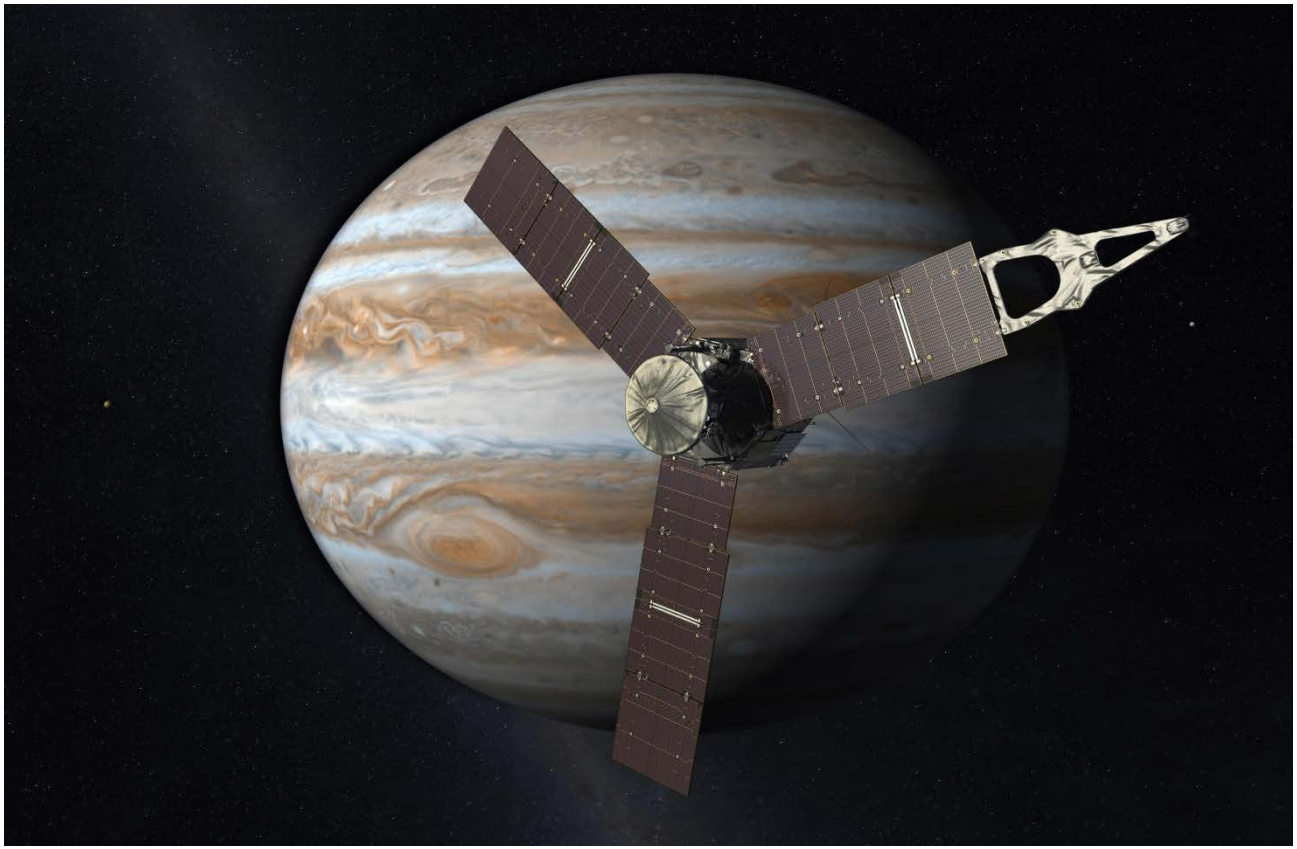


Capabilities with hardware RAD750

- ITC can execute VxWorks and RTEMS operating systems on the RAD750 platforms
- ITC can recompile and target sections of mission code that require analysis
- ITC is currently building a 1553 and SpaceWire capability to interface with external systems including Software Models

Use Case

- Juno Anomaly

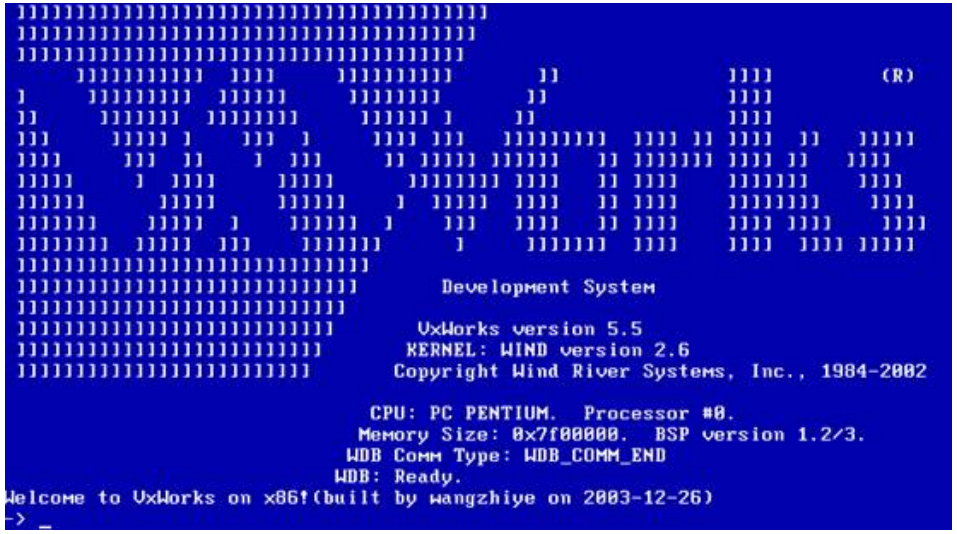


Problem

- Juno had a condition where the processor raised an ISI exception
- Unique to this condition was that the exception kept getting raised at 10Hz instead of the task suspending
- Eventually a system monitor switched sides because the faulting task was not reporting good health

Analysis

- JPL requested that IV&V try to reproduce the repeated exception behavior
  - Believed to be an OS issue in Task Control Block
- The ITC software environment would not recreate the ISI exception
- Moved VxWorks 6.4 image to RAD750 with test application



Results

- Through specific manipulation of the VxWorks Task Control Block, ITC was able to achieve a cyclic ISI behavior on the RAD750 target
- This information was conveyed back to the contractor so they could focus their analysis
- Ultimately the project determined the fault to be a “fluke” and no corrective action was taken

Conclusion

- There are many tools and methods required to provide successful software IV&V
- Static analysis and Dynamic analysis with software models are major players
- However, there will always be cases where flight equivalent hardware is needed to validate and verify specific software behaviors and anomalies

Contact Information

- Web Page
  - http://www.nasa.gov/centers/ivv/jstar/JSTAR.html
- E-Mail
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- Contact us for…
  - Demonstrations of test beds
  - Middleware usage agreements
  - Simulator development
  - Hardware modeling
  - V&V Services, HWIL Testing, Performance Testing