estimate

estimate • analyze • plan • control

Bottoms Up Estimating of NASA Instruments Using Technical Parameters

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About Galorath

Galorath's consultants and SEER products help clients estimate effort, duration, cost, and gauge risk

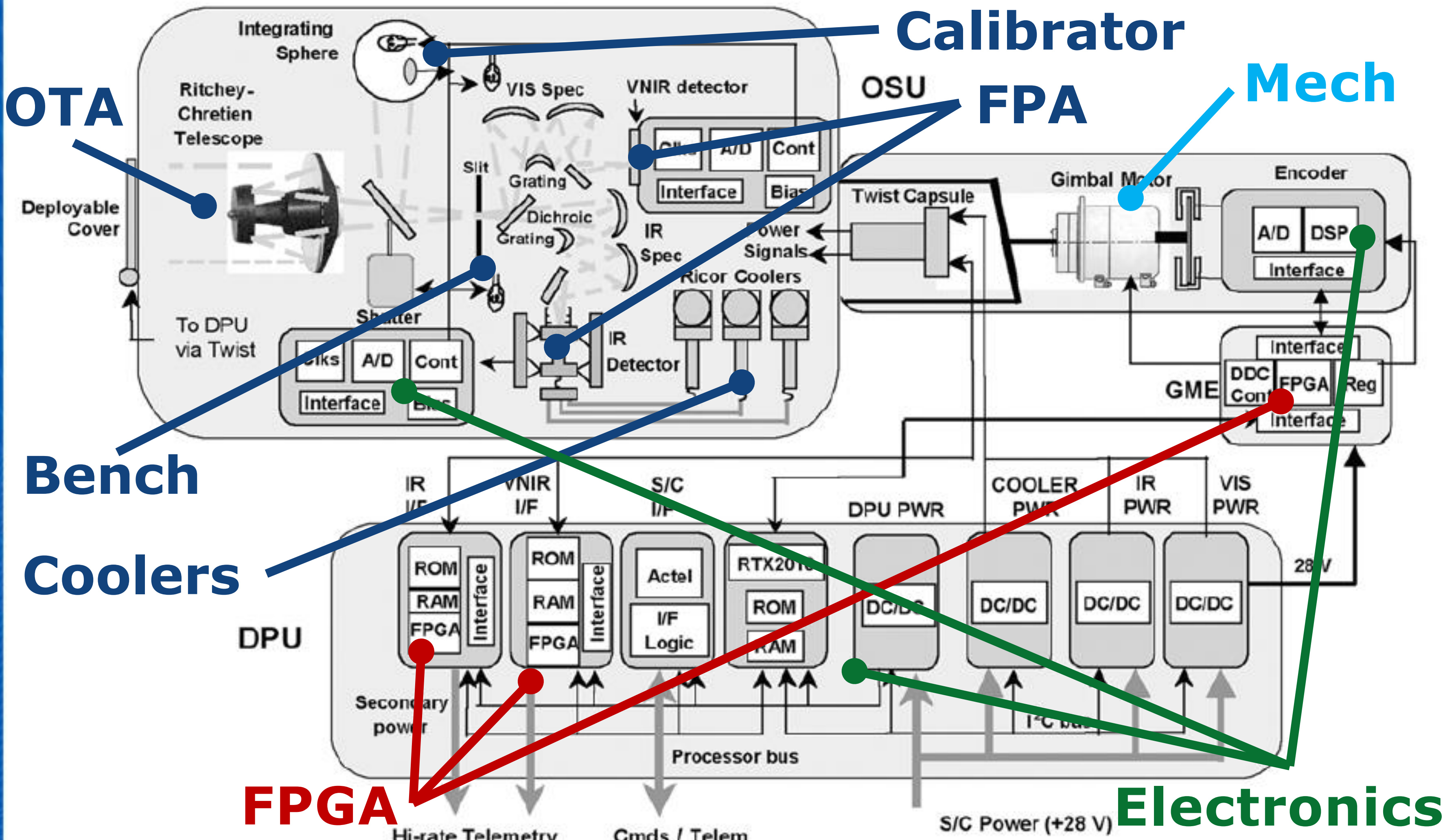
- Over 30 years in business conducting mil/aero cost research
- Hundreds of customers, many Fortune 500
- Small business (NAICS 541330, 541511, 541611, 541712)
- Professional services organization provides consulting and training
  - Supporting NASA with ~15 cost estimators
  - Over 100 unique instruments estimated for NASA during the last 2-3 years
- A software publisher / research firm with four flagship products:

Background – Estimating with Technical Parameters

- Our research into the relationships between technical parameters and cost began more than 10 years ago (first released Spyglass during December 2004)
- Two areas where we have achieved greatest maturity:
  - Electro-optical systems in Space, Aircraft, and Missile platforms
  - Integrated Circuits (printed circuit boards, FPGAs and ASICs)
- Our methodology utilizes 3 to 8 Key Technical/ Performance Parameters (KTPPs) for each technology (i.e., device or process) estimated
  - Applying quantitative analysis that simultaneously solves capability vs. cost assessments
  - Estimates at the component and assembly levels

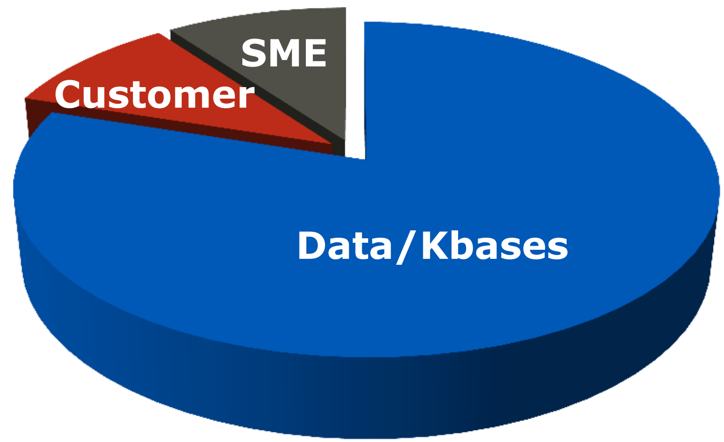
Example – CRISM on MRO

- All of the instrument elements identified below are estimated based on key technical and performance parameters



Citation: Murchie, S., et al. (2007), Compact Reconnaissance Imaging Spectrometer for Mars (CRISM) on Mars Reconnaissance Orbiter (MRO), J. Geophys. Res., 112, E05S03, doi:10.1029/2006JE002682.

What Drives the Technical Foundation of the Models?



- Data purchased, some donated. Data includes cost and technical information
- SMEs support creation of architecture and mapping of parameters
- Routinely work with customers in ongoing validation of model
- Most information is from MIL/AERO sources
- Some validation of models comes from indirect methods. Online prototype to foster analysis and review
- Conduct Capabilities Review Meetings with customers
- Models target "middle of the road" scenarios with ability to adjust to individual environments
- Continuously do research and releases are about every 18 months

Subject Matter Experts

- Galorath augments its staff with external technical SMEs
  - Program Director (Ford/Loral) – 35 years experience in managing space programs
  - Program Manager (Perkin Elmer) – 32 years experience in managing EOS programs for space applications
  - Product Line Director (Honeywell/Bendix Space Systems) – 27 years experience in mechanisms for space applications
  - Senior Scientist (Barnes Engineering/EDO/Goodrich) – 30 years developing electro-optical systems for commercial and space applications
  - Product Line Manager/Business Development (Honeywell/SAIC) – 25 years development of advanced IR focal plane arrays and related business development
  - Chief Engineer (Honeywell Space Systems) – 16 years development of advanced mechanisms and control systems

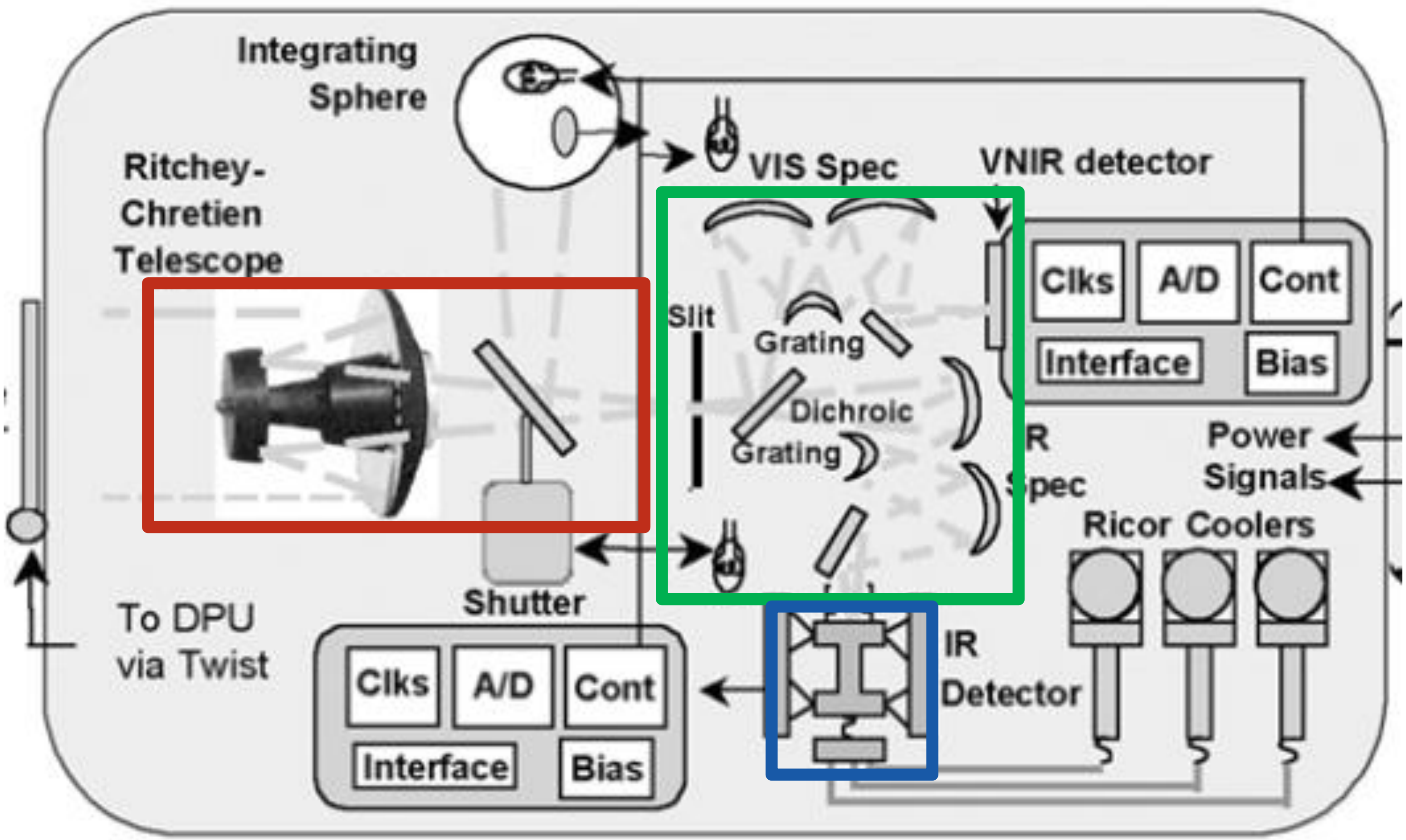
ESTIMATING ELECTRO-OPTICAL SENSORS UTILIZING KTTPS

Example EOS Key Technical/ Performance Parameters

- Reflective Telescope
  - Imaging Elements
  - Non-Imaging Elements
  - Largest Element Diameter
  - Optic Surface Quality
  - Imaging Optic Surface Shape
  - Structure / Optic Material
- Area Silicon CCD
  - Array Size (Pixels)
  - Frame Rate
  - Readout Noise
  - Radiation Tolerance
  - Pitch
- Single Stage Reverse Brayton
  - Cooling Load
  - Max Delta Temperature
  - Mission Life
- Mirror Scan Drive Assembly
  - Resolution
  - Accuracy
  - Number of Axes
  - Torque
- Acceptance Testing
  - Detector Arrays
  - Spectral Bands
  - Thermal Plateaus
  - Primary Optic Diameter
- Laser Diode
  - Array Size
  - Max Optical Output Power
  - Cooling Required
  - Laser Diode Chip Material

Example – Compact Reconnaissance Imaging Spectrometer for Mars

- We will examine the telescope, optical bench and a detector in more detail



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Example Methodology - Detector

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1. Each cost element has a set of "technologies"

Area HgCdTe

- !No Knowledge
- Area Bicolor HgCdTe
- Area HgCdTe
- Area HgCdTe APD
- Area InGaAs
- Area InSb
- Area Microbolometer
- Area Si CCD
- Ge:Ga or Si:Ga Photoconductor
- Linear Gallium Nitride
- Linear HgCdTe
- Linear HgCdTe APD
- Linear InGaAs
- Linear InSb
- Linear Si CCD
- Linear Si Detector

2. The selected technology determines the KTPPs

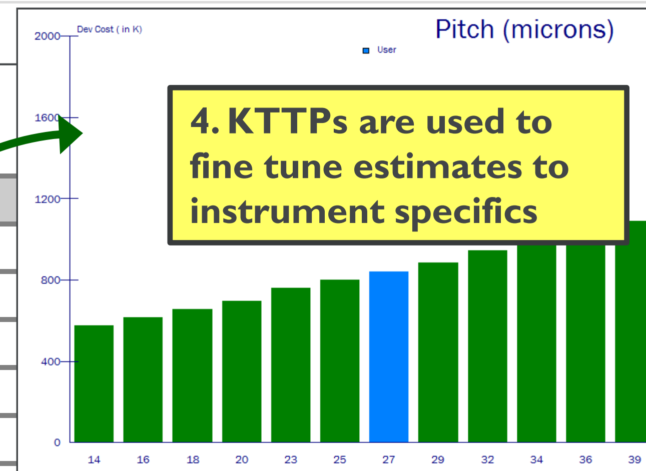
EOS Detector: IR		Likely
PRODUCT D...		
Technology		Area HgCdTe
KEY TECHNICAL/PERFOR...		
Array Size (pixels)	307,200	307,200
Rows (pixels)	480	480
Columns (pixels)	640	640
Radiation Tolerance (rad)	7,200	8,000
Cutoff Wavelength (microns)	314.96	393.70
Dead Pixels	0.40%	0.50%
Pitch (microns)	27	27
PROGRAM DESCRIPTION		
New Design	10.00%	15.00%
Design Replication	0.00%	0.00%
Design Complexity		

Pitch

The pixel center-to-center spacing.

Technology:	Minimum	Maximum
Area Bicolor HgCdTe	20	50
Area HgCdTe	14	56
Area HgCdTe APD	40	200
Area InGa...	14	56
Area InSb	14	56
Area Micro...	25	150

3. KTPPs influence functions set baseline cost sensitivities



4. KTTPs are used to fine tune estimates to instrument specifics

CRISM Optical Telescope Assembly

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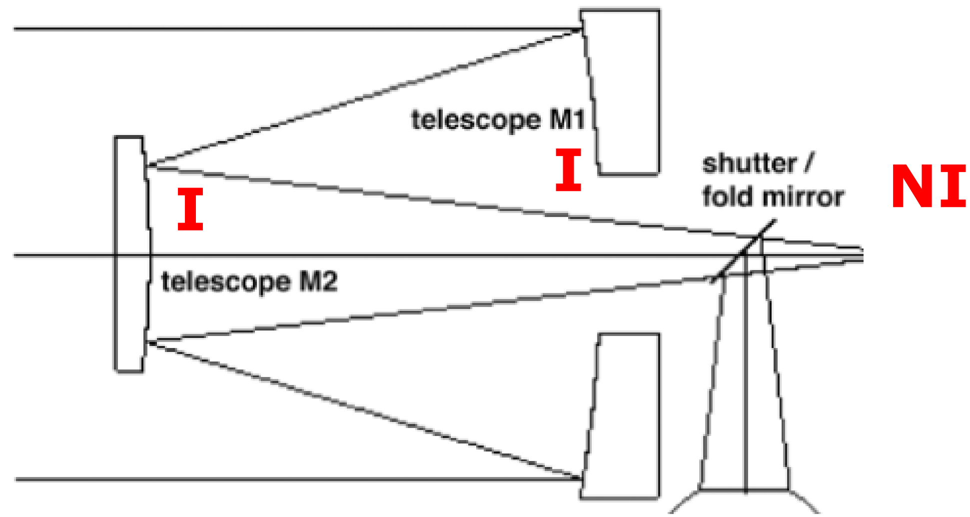
- Ritchy-Chretien telescopes are reflective
- M1 Diameter: 10 cm from supporting technical documentation
- Material: Aluminum



EOS Optical Device: Ritchy-Chretien Telescope	Least	Likely	Most
PRODUCT DESCRIPTION			
Technology		Reflective Telescope	
KEY TECHNICAL/PERFORMANCE PARAMETERS			
Imaging Elements	2	2	2
Non-Imaging Elements	1	1	1
Largest Element Diameter (cm)	10.00	10.00	10.00
Imaging Optic Surface Shape		Spherical	
Structure/Optic Material		Standard	
Surface Accuracy	20	20	20

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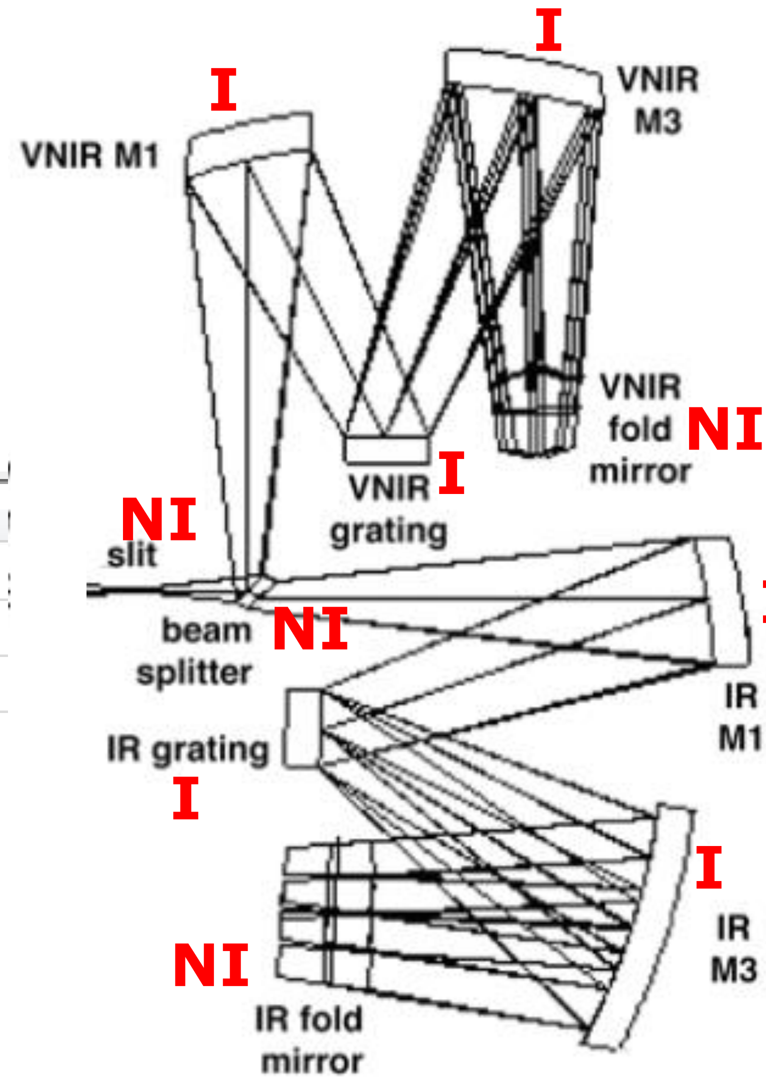
CRISM Optical Bench

EOS Optical Device: Optical Bench	Likely
Imaging Elements	6
Non-Imaging Elements	4
Collecting Aperture (cm²)	16.00
Optical Bench Material	Aluminum Honeycomb

Note
4 Mirrors (2 VNIR, 2 IR), 2 Gratings
Spectograph Entrance Slit, Dichroic Beamsplitter, 2 Fold Mirrors
Assumes radius of 2.25cm for M1 mirror on the optical bench.

- Note: In the future gratings will become stand-alone cost elements



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Examples of Technologies Estimated

Optical Devices	
Camera Optical Assemblies or Optical Benches	Lenses – Aspherical, Spherical, Conical
Astronomical Telescopes	Refractive Telescopes – IR and Visible
Reflective Telescopes	Mirrors – Standard and Lightweight Options for Aspherical, Spherical, Conical
Filters – Broad Band, Long Wave, Narrow Band, Short Wave	

Detectors	
Large Linear or Silicon CCD	Area HgCdTe (Hi/Lo Rad, APD, Bicolor)
Linear Silicon Detector	Linear or Area InSb
Linear Gallium Nitride	Ge:Ga or Si:Ga Photoconductor
Multi-Anode Micro Channel (MAMA)	Linear or Area InGaAs
Linear HgCdTe (Hi/Lo Rad, APD)	Area Mircobolometer

Lasers	
Laser Diode (Active,Passive, No Cooling; QWIP, AlGaAs, InGaAs Chip)	Diode Pumped NdYAG Lasers (Active, Passive Cooling)

Examples of Technologies Estimated (Continued)

Coolers	
Single Stage Thermoelectric	Multistage Sorption
Two Stage Thermoelectric	Single Stage Reverse Brayton
Single Stage Sterling or Pulse Tube	Two Stage Reverse Brayton
Two Stage Sterling or Pulse Tube	Joule-Thompson (w/wo) Pressure Vessel

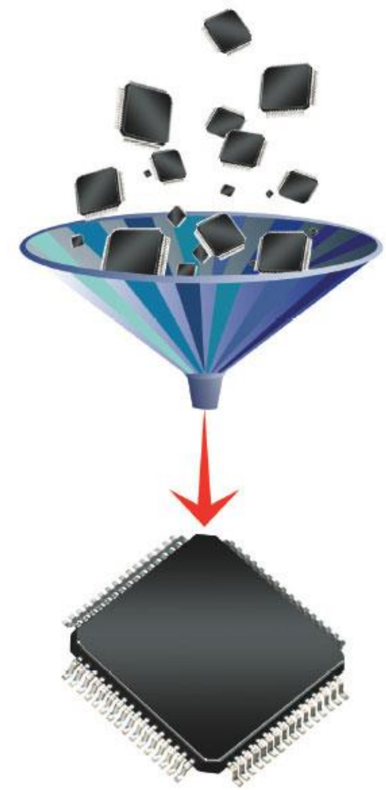
Mechanisms	
Mirror Scan Drive Assembly	Alignment Assembly
Fast Steering Mirror	One-axis Piezoelectric Actuator
Selectable Optical Filter Assembly	Gimbal

Calibrators	
Visible/NIR Integrating Sphere	Geometrically Enhanced Blackbody
Optical Cavity Blackbody	Collimated Blackbody Source

ESTIMATING INTEGRATED CIRCUITS & ELECTRONICS UTILIZING KTTPS

Why bother with electronics KTTP?

- There are challenges when doing analysis of alternatives between electronic subsystems by just looking at power or weight.
- The capability of electronics is continuing to get more complex. Field Programmable Gated Arrays (FPGAs) and ASICs continue to grow in capability.
- If the satellite requires more real-time processing, the electronics will grow in complexity. Common for years on DoD systems. Increasing on Science missions.



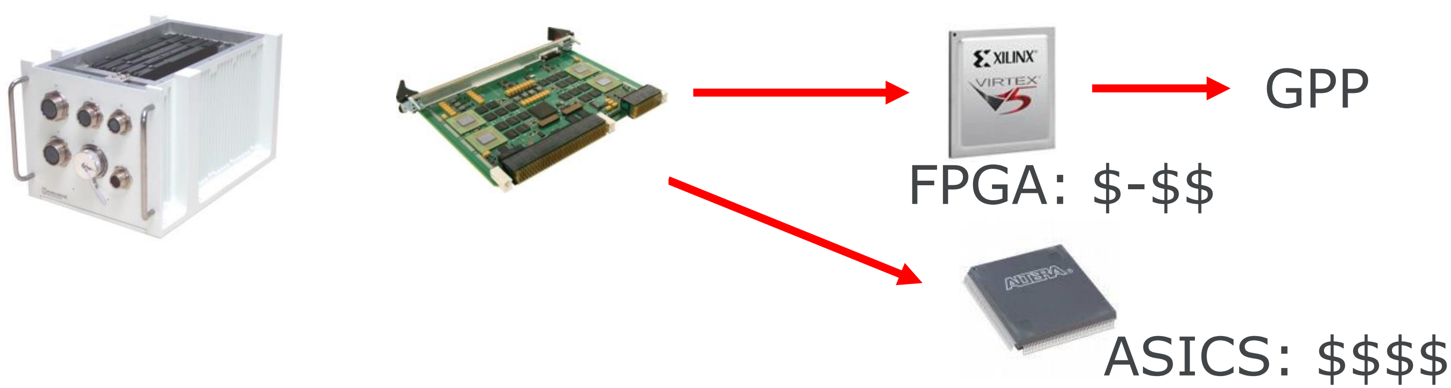
Example Technology Characterization

Method / Category	FPGA	Gate Arrays or Structured Cell	Standard Cell	Full Custom	System on a Chip
Electronic Design Automation (EDA)$	Low	Low +	Med	High	Very High
Schedule	Low	Low+	Med	High	Very Long
Power Consumed	High	High+	Med	Low	Low
Speed	Low	Low+	Med	High	High
Requirement Volatility	Very Flexible	Flexible	Need Stability	Large Hit for design mod	Vlarge Hit for design mod
Mask Costs	None	None	Med-High	Very High	Very High
Development $	Low	Low+	Med-High	Very High	Very High
Die Size (Recurring $)	Purchased die (commodity)	Purchased die (commodity)	Low	Best	Good

Digital Electronics Example

Standard board, General Purpose Processors (GPP) with software

Smaller, less weight, more capable, BUT more complex, $$$$



Example IC Key Technical/ Performance Parameters

- Printed Circuit Board
  - Function/Application
  - Size (mm^2)
  - Substrate Material
  - Circuitry Composition
  - I/O Counts
  - Clock Speed
- Field Programmable Gate Array
  - Function/Application
  - Material Classification
  - Speed Grade
  - Feature Size (nanometers)
  - Active IO Pins Per Chip
  - Clock Speed (MHz)
  - Effective Logic Cells
    - Logic Cells
    - IP Logic Cells
    - Memory (Mbits)
    - System Gates, etc.
- ASIC
  - Function/Application
  - Technology
  - Process
  - Die Area (mm^2)
  - Feature Size (nanometers)
  - Effective Gates Per Chip
    - Logic Gates
    - Memory Gates
    - Etc.
  - Active IO Pins Per Die
  - Clock Speed (MHz)
  - Wafer Diameter (mm)
  - Package Type
  - Radiation Level

FPGA Example Using KTTPs

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KEY TECHNICAL/PERFORMANCE PARAMETERS			
Material Classification		HP Signal Processing	
Speed Grade		High	
Feature Size (nanometers)		65	
Active IO Pins Per Chip	417	501	584
Clock Speed (MHz)	170.00	200.00	230.00
Effective Logic Cells		120,252	
Logic Cells	65,535	78,642	91,749
Logic Cells Complexity	Nom-	Nom	Nom+
IP Logic Cells	0	0	0
IP Logic Cells Complexity	Nom-	Nom	Nom+
Memory (Mbits)	5.24	6.29	7.34
Memory (Mbits) Complexity	Nom-	Nom	Nom+
Additional Sizing Parameters			
System Gates	0	0	0
Logic Elements	0	0	0
Multipliers	0	0	0
Transceivers	0	0	0
Flip Flops	0	0	0
DSP Blocks	160	192	224
Proxy Unit X	0	0	0
Proxy Unit X Factor	0	0	0
PROGRAM DESCRIPTION			
New Design	55.00%	65.00%	70.00%
Design Replication	0.00%	0.00%	0.00%
Utilization	50.00%	60.00%	70.00%

Feature Size set

Chip resources set according to utilization percentage including a range for uncertainty (case shown is assuming 50%, 60%, 70%)

Based on Xilinx Virtex-5QV Family Overview, http://www.xilinx.com/support/documentation/data_sheets/ds192_V5QV_Device_Overview.pdf

FPGA Example of Excursions

- Excursions can help identify the cost impacts of different nonrecurring engineering and KTTP utilization assumptions, for example

	Average Modification		Major Modification	
	60% Utilization	80% Utilization	60% Utilization	80% Utilization
Activity				
Architectural Design	196,566	261,136	293,314	389,664
Design Capture	239,585	318,285	357,506	474,943
Layout, Place and Route	43,550	57,856	64,985	86,332
Verification	359,196	477,188	535,990	712,056
Prototype Development	87,078	115,682	129,937	172,620
Integration and Test	163,271	216,904	243,632	323,662
Program Management	194,306	258,133	289,942	385,184
Total Development Cost	1,283,552	1,705,184	1,915,306	2,544,461

Trade Study/Scenario Example

- A combination of KTTPs and component level labor and materials detail enables meaningful trade studies and/or scenario development

- **KTTPs Populated**
  - Application: Signal Processing
  - Technology: Standard Cell
  - Process: CMOS
  - Die Area: 3mm^2
  - Feature Size (nanometers): 65
  - Logic Gates: 550K
  - Clock Speed (MHz): 2,000 (i.e. 2 GHz)

Signal Processing ASIC Development	Minor Modification Scenario		Single Re-Spin Scenario		
Activity/Material	**Labor**	**Materials**	**Factor**	**Labor**	**Materials**
IC Requirements Definition	$ 770,147	$ -	0%	$ -	$ -
Front End Design Effort	$ 2,163,502	$ -	0%	$ -	$ -
Back End Design Effort	$ 3,926,442	$ -	0%	$ -	$ -
Re-Spin Effort	N/A	$ -	N/A	$ 634,732	$ -
Mask Sets	$ -	$ 2,534,401	20%	$ -	$ 506,880
Prototype Run	$ -	$ 330,952	100%	$ -	$ 330,952
Total Cost	$ 6,860,091	$ 2,865,353		$ 634,732	$ 837,832

Estimate Range: $1.5M - $10M

Validation

- Continually doing validation with our customers. Even when data is not provided, we receive feedback on cost outputs and parameter weight/sensitivity
- Supports understanding on how component level modeling could be done better or identify new key technical parameters
- Customers champions also support the creation of new Knowledge base defaults.
- Formal validation of model based on specific cost data. Must have solid understanding of not only the cost output but also what drove it (technically, programmatically, etc.). Cost forensics.

Challenges

- Technical understanding to interpret diagrams and associated narratives at the component level
- Lack of a Master Equipment List and/or detailed diagrams significantly impacts modeling accuracy. The models do not readily support system or subsystem level estimating.
- Technical parameters are not always given and the analyst must calculate or derive these values
- Component/assembly level estimating requires more time and effort than top-down approaches
- Reliance on strong industry/developer relationships because Government data is frequently high level
- Technical characterization of the tremendous variety of science sensors and instrumentation

What We Are Working On Now

- 2^{nd} formal model validation study with NASA
- Mass Spectrometers
- Particle Counters
- Cubesats
- Platform-driven cost impacts (e.g. ISS)
- Gratings as individual cost elements
- Cross delay line (XDL) detectors
- Micro-channel plate (MCP) detectors
- EOS cost impact of X-ray and gamma ray wavelength missions
- Laser spectroscopy

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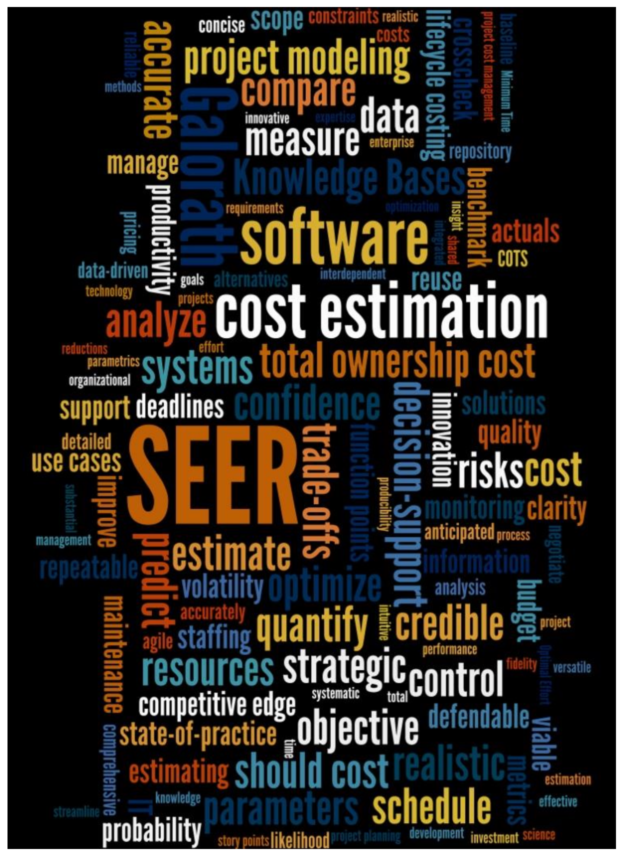

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