

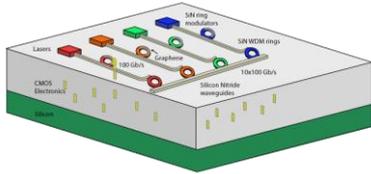


Ultra-Low Power CMOS-compatible Integrated Photonic Platform for Terabit-Scale Communications



Team

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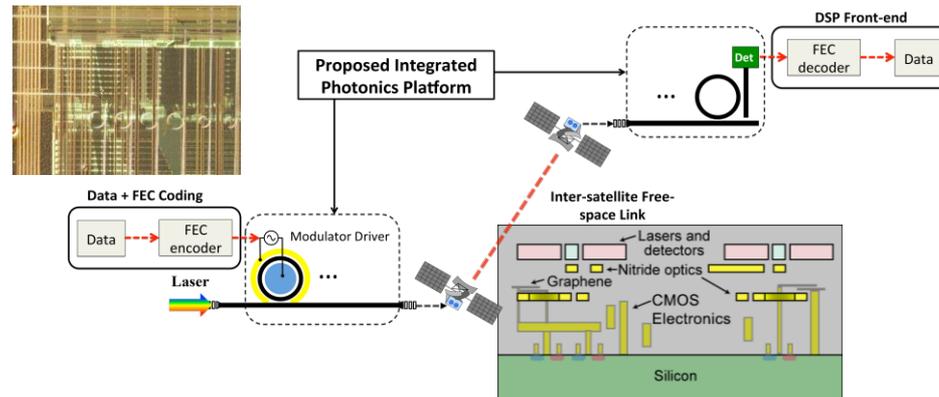
Research Objectives

- Current state-of-the-art free space laser links at telecommunications wavelengths are limited in bandwidth to < 1Gbps mainly due to the high energy consumption of optical transceivers.
- Realize fully CMOS-compatible platform for ultra-low power Terabit-scale optical communications
- Optical space communication of user-programmable variable data rates ranging from 10's of MHz to 100's of GHz within the critical ultra low power (1–10W) envelope
- Build complete suite of fabrication and simulation tools needed to integrate and design photonics and electronics components in 3D CMOS-compatible platform
- Demonstrate fully operational free space link **with variable bandwidth from 10Mbps to 100Gbps** and forward error correction under 10W total power consumption

Approach

- Novel **3D deposited nanophotonic platform**. Enables complex photonics devices combining modulators, detectors, switches, waveguides, lasers, and routers with **full and seamless integration with CMOS electronics**
- Fabrication of photonic structures directly **on top** of standard CMOS electronics
- 3D integration of active photonics: TRL 1 at program initiation to TRL 3.

Ultra-low power Terabit-Scale Optical Communications



Potential Impact

- **Ultrafast data upload/download** to revolutionize scientific instrumentation in space
- **Ultra-low power, high speed communications** enables inter-satellite communications networks
- **Dramatic decrease** in size, mass, and power consumption
- Drastically reduced power consumption for broad optical communications and large data networking

Ultralow power 100's GHz transceiver based on monolithically integrated photonic devices with state of the art CMOS electronics. Bottom right: 3D photonics platform integrated directly on the CMOS. Top Left: Preliminary results demonstrating monolithically integrated silicon nitride rings within 90nm process CMOS die. (photonic ring components and the metal vias visible underneath)