National Aeronautics and
Space Administration

Mary W. Jackson NASA Headquarters
Washington, DC 20546-0001

February 16, 2022

Reply to Attn of: Office of International and Interagency Relations

Dr. Alan Baratz
Chief Executive Officer
D-Wave Systems Inc.
3033 Beta Avenue
Burnaby, British Columbia
V5C 4M9 Canada

Dear Dr. Baratz:

The purpose of this letter is to amend and extend the reimbursable Space Act Agreement between the National Aeronautics and Space Administration (NASA) and D-Wave Systems Inc., hereinafter jointly referred to as "the Parties," for adiabatic quantum computing fabrication process development, hereinafter referred to as the "Agreement." This Agreement entered into force on June 22, 2011. The Agreement was amended and extended on July 31, 2014, September 25, 2017, and November 8, 2019.

I propose to amend and extend the Agreement as follows:

1. **Recognition of JPL Task Plan Change:**

Due to the change in the JPL Task Plan to accommodate the extension and amendment of the Agreement, the words "JPL Task Plan No. 97-16404, Revision E," are to replace all references to the JPL Task Plan in the Agreement. In addition, the Agreement's attachment of JPL Task Plan No. 82-16404, Revision D is to be replaced with JPL Task Plan No. 97-16404, Revision E, which is enclosed.

2. **Key Personnel**

NASA proposes to delete the Business/Administrative Points of Contacts under Article 22, Key Personnel, and replace as follows:

"Business/Administrative Points of Contact

NASA	**D-Wave Systems Inc.**
Nar Nazari Contracting Officer NASA Management Office 4800 Oak Grove Drive Pasadena, CA 99 IO 19 U.S.A. Telephone: (818) 354.5619 Email: nar.r.nazari@nasa.gov	Alan Baratz Chief Executive Officer 3033 Beta Avenue Burnaby, BC V5G4M9 Canada Telephone: 604-630-1428 ext. 110 Email: abaratz@dwavesys.com"

3. Term of Agreement

NASA proposes to delete Article 18, "Term of Agreement," in its entirety and replace it with the following:

> "This Agreement becomes effective upon the date of the last signature below and shall remain in effect until the earlier of the completion of all obligations of both Parties hereto or August 31, 2027."

4. Article Numbering in Previous Amendments

For the avoidance of doubt, NASA proposes to replace references to "Article 5, 'Financial Obligations'" with "Article 6, 'Financial Obligations'" in the amendments to this Agreement concluded on September 25, 2017 and November 8, 2019.

If the above terms and conditions are acceptable to D-Wave Systems Inc., I propose that this letter, together with your affirmative reply, constitutes an amendment and extension to our Agreement that will enter into force on the date of your reply.

Sincerely,

KENT BRESS Digitally signed by KENT BRESS
Date: 2022.02.16 15:31:46
-05'00'

Kent Bress
Director, Aeronautics and Cross-
Agency Support Division

Enclosure

Confirmed on behalf of D-Wave Systems Inc.

DocuSigned by:
Alan Baratz
14309ACD421C41F...
CEO
17-Feb-2022 | 1:15 PM PST

ADIABATIC QUANTUM COMPUTING FABRICATION PROCESS DEVELOPMENT

to

D-Wave Systems Inc.
3033 Beta Ave.
Burnaby, BC V5G 4M9 Canada

JPL Task Plan No. 97-16404, **Revision E**

JET PROPULSION LABORATORY
California Institute of Technology
Pasadena, California 91109

REVISION LOG

Revision	Change	Executed
A	Revision A supported the development of an Adiabatic Quantum Computing (AQC) approach to solving complex optimization problems by extending the contract by three years through September 30, 2017 and increasing the contract value by $1,022,437. As a result, the total cost estimate increased by $1,022,437 from $2,556,093 to $3,578,530.	29-July-2014
B	Revision B supported the continuation of developing an Adiabatic Quantum Computing (AQC) approach to solving complex optimization problems by JPL handling fabrication and diagnostic characterization in support of D-Wave's process development while D-Wave handles circuit designs and functional testing. As a result of this continuation, Revision B increased the contract value by $690,100. As a result, the total cost estimate was increased from $3,578,530 to $4,268,631.	9-November-2015
C	Revision C is to support the development of an Adiabatic Quantum Computing (AQC) approach to solving complex optimization problems. JPL will continue to handle fabrication and diagnostic characterization in support of D-Wave's process development while D-Wave continues to handle fabrication process development and circuit designs and functional testing As a result of this modification, the Programmatic Cost Estimate is increased from $4,268,631 by $1,839,285 to $6,107,916 (Including NASA Cost). For informational purposes, the NNN12AA01C contract value is $3,366,691 (Excluding NASA Cost). The Programmatic Period of Performance will be June 22, 2011 through September 29, 2019. Upon execution of this Revision C, the Contractual Period of Performance will be October 1, 2012 through September 30, 2018. All Revision C changes are shown in bold.	25-September-2017

REVISION LOG, cont.

Revision	Change	Executed
D	The purpose of this Task Plan, Revision D, is to note the new NASA Prime Contract and a change in the JPL Program Office oversight. The Task Plan, Revision D, will continue to authorize support of the development of an Adiabatic Quantum Computing (AQC) approach to solving complex optimization problems. JPL will continue to handle fabrication and diagnostic characterization in support of D-Wave's process development while D-Wave continues to handle fabrication process development and circuit designs and functional testing. As a result of this modification, the Cost Estimate is increased from $5,825,650 by $2,268,813 to $8,094,463 (excluding NASA Cost). For informational purposes, the Lifecycle Value is increased from $6,107,916 by $2,436,862 to $8,544,778 (including NASA Cost). The Period of Performance is extended thirty-six (36) months beyond the current 29-September-2019 end-date to 24-September-2022. The Lifecycle Period of Performance will be 22-June-2011 through 24-September-2022. TP 97-16404, Revision D, replaces in its entirety TP 82-16404, Basic, as amended through Revision C.	31-October-2019
E	The purpose of this Task Plan Revision E is to extend the existing period of performance through August 31, 2027. There is no change to the cost estimate, which remains $8,544,778 (including NASA cost), nor scope of work. Milestones and deliverable dates are adjusted according to the new schedule.	17-Jun-21

Note: Significant changes indicated in red text.

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A. INTRODUCTION

1. BACKGROUND

Advanced computer technology is critical to supporting JPL mission objectives. In particular, combinatorial optimization represents a problem class of central importance that pervades mission planning, engineering design, robotics and artificial intelligence. D-Wave Systems Inc. (hereinafter referred to as "D-Wave") is developing Adiabatic Quantum Computing (AQC) as an approach to solving complex optimization problems by encoding data in arrays of Superconducting Quantum Interference Devices (SQUIDs) that act as quantum bits (qubits). The system remains in its ground state while adiabatically evolving from a simple, known configuration to a final configuration that provides the answer to the computational problem of interest. D-Wave has made numerous demonstrations of prototype AQC processors, which are projected to outperform conventional supercomputers by a wide margin within a handful of years.

JPL and D-Wave began a highly successful collaboration in 2005 under JPL Task Plan 82-10225, "Nb Quantum Computing" (Task Order NMO715801). The collaboration expanded in 2007 under JPL Task Plan 82-11375, "Nb Quantum Computing Circuit Fabrication" (Task Order NMO715967). Task Plan 82-11375 ended on June 26, 2011. Both D-Wave and JPL continued their successful collaboration through September 30, 2014 under this follow-on Task Plan, 82-16404. The nature and scope of the follow-on work described here are very similar to the work involved in Task Plan 82-11375.

Beginning in 2005, the JPL Microdevices Lab (MDL) fabricated prototype circuits and processor chips for D-Wave, beginning with single devices and individual qubits. By late 2007, D-Wave was solving benchmark problems using a 28 qubit processor fabricated at JPL, enabling a critical experimental examination of the AQC approach and the beginning of scaling studies of computational power with the number of qubits in the array. In parallel, D-Wave and JPL developed classical superconducting circuitry to control the quantum circuits. In these collaborative efforts, JPL was the sole source of quantum hardware for D-Wave, handling process development, fabrication, and initial characterization while D-Wave handled circuit designs and functional testing.

By 2008, in anticipation of eventual commercial success and with technical support from JPL, D-Wave had developed its own chip manufacturing capability. Through 2012, D-Wave produced complex superconducting quantum annealing processor chips at SVTC, a commercial Complementary Metal Oxide Semiconductor (CMOS) circuit foundry in San Jose, CA. In 2012, SVTC ceased operations and D-Wave transferred its process to Cypress Semiconductor in Bloomington, MN. The availability of this process, arguably the most advanced superconductor process in the world, has allowed D-Wave to fabricate and yield quantum annealing processor chips containing over 2000 qubits and 300,000 Josephson junctions. These are the most complex superconducting chips currently ever produced anywhere in the world. D-Wave has to continue to advance its process in order to meet new goals. Achieving future goals will require continuous process improvement. To that end, JPL remains an essential partner of D-Wave.

In a modern CMOS foundry, troubleshooting typical fabrication-related problems and introducing new materials and processes is costly and time-consuming. Fabricating superconductor circuits in such a facility introduces additional difficulties, as some essential materials and processes are non-standard. Although the benefits of operating a non-standard process in such a facility outweigh the costs, D-Wave's experience has taught that running, maintaining, and advancing its superconductor process requires close collaboration with an R&D facility operating in a rapid prototyping mode. This role has been filled by JPL, and D-Wave regards continued collaboration with JPL as essential to its success. This Task Plan defines for JPL a continuing R&D role that emphasizes support for D-Wave's manufacturing process development, rapid prototyping of advanced designs, new circuit approaches, and fundamental physical investigations.

During the previous years of this effort, much was accomplished:

- Process development
  - JPL diagnostic measurements and analysis enabled D-Wave to mitigate several problems related to excessive heating of wafers containing Josephson junctions during the fabrication process. JPL continues to support fabrication process development with diagnostic measurements and analysis and with process-related experiments.
  - D-Wave and JPL have expanded this capability via additional sub-4 K measurement infrastructure at JPL. (A sub-4 K measurement means that the sample being tested is at a temperature of 4 degrees above absolute zero or colder.)
  - JPL has led experimental work that has enabled D-Wave to establish a high-critical current density (J_c = 10 kA/cm^2) process. This is enabling D-Wave to add a second junction layer to its process. It also allows D-Wave to supply wafers for classical single flux quantum computing circuits for anticipated government and commercial projects.
  - JPL has continued to lead in the analysis of the high-Jc process. JPL made significant advances in implementing and understanding the use of room temperature device resistance measurements as a proxy for cryogenic critical supercurrent measurements at millikelvin temperatures. In particular, JPL developed corrections for parasitic device resistance at room temperature that allow the measurements to be applied to high-J_c wafers. This resulted in a joint publication [Alan W. Kleinsasser, Talso Chui, Bruce Bumble, and Eric G. Ladizinsky, "Critical Current Density and Temperature Dependence of Nb-Al Oxide-Nb Junction Resistance and Implications for Room Temperature Characterization", *IEEE Trans. Appl. Supercond.* Vol. 23, Article 1100405, June 2013]. JPL continues to support improved room temperature characterization of high-Jc devices.
  - JPL has carried out several fabrication experiments to test new circuit-related ideas. For example, in 2015, JPL fabricated chips that were successfully used by D-Wave to establish a new resonator-based approach to qubit readout. [J. D. Whittaker, L. J. Swenson, M. H. Volkmann, P. Spear, F. Altomare, A. J.

Berkley, B. Bumble, P. Bunyk, P. K. Day, B. H. Eom, R. Harris, J. P. Hilton, E. Hoskinson, M. W. Johnson, A. Kleinsasser, E. Ladizinsky, T. Lanting, T. Oh, I. Perminov, E. Tolkacheva, and J. Yao, "A frequency and sensitivity tunable microresonator array for high-speed quantum processor readout," *J. Appl. Phys.* Vol.119, Article 014506, January 7, 2016.]

- D-Wave process transfer
  - D-Wave's circuit manufacturing process was carried out at SVTC in San Jose, CA from 2008 – 2012. In September 2012, SVTC suddenly announced that it would cease operations by the end of the year. D-Wave transferred its process to Cypress Semiconductor in Bloomington, MN in early 2013. **The new process is fully operational and has yielded the first functional 2000-qubit quantum annealing chips.** JPL provided much essential technical support during the transfer and in bringing up the process at Cypress. For example, JPL measurements and analysis were essential in establishing a new Nb deposition in a Cypress Endura cluster deposition system and in re-establishing, and advancing, the D-Wave trilayer Josephson junction growth process in its relocated Axcela cluster tool (e.g., studying feasibility of tunnel barrier growth in the ICP chamber for better uniformity and reproducibility and mapping out R_nA vs. exposure and junction quality vs. R_nA).

- JPL SQUID-based 1/f noise measurements
  - In FY 2013, JPL built a cryogenic probe to perform for 1/f noise measurements at 4 K on Superconducting Quantum Interference Devices (SQUIDs). JPL then worked with D-Wave to establish the relationship between these results and more cumbersome macroscopic resonant tunneling measurements at D-Wave.
  - In FY 2014, JPL extended its SQUID measurements to mK temperatures.
  - In FY 2015, JPL established 1/f flux noise measurements based on flux bias reversal and carried out experiments to demonstrate that 4 K measurements can be used as a proxy to characterize noise at mK base temperature.
  - In 2017 JPL and D-Wave designed new test chips for experiments involving fabrication at both JPL and D-Wave.

- JPL broadband noise measurements
  - Beginning in FY 2013, JPL demonstrated, and has continued to conduct, lumped element (L-C) and microstrip resonator-based broadband noise measurements at mK temperatures on D-Wave chips.
  - JPL and D-Wave designed new test chips with D-Wave for experiments involving fabrication at both JPL and D-Wave.
  - These ongoing experiments have been an outstanding success. For example, this capability was important for establishing the aforementioned resonator-based qubit readout scheme.
  - In FY 2015, JPL upgraded its measurement capability in order to triple the number of resonator chips it can measure in a single dilution refrigerator cooldown. JPL has carried out resonator noise measurements at mK temperatures at the rate of roughly one cooldown every six weeks and plans to continue at that rate.

Successes in this Task led D-Wave and JPL to extend the original Task Plan through Fiscal Year 2019 (revisions A, B, and C). JPL 1/f and broadband noise measurements enabled by the previous revisions led to a fundamental re-appraisal of D-Wave's understanding of noise in their qubits at frequencies ranging from below 1 Hz into the GHz regime. JPL extended this measurement capability during Task Plan Revision D.

With this Task Plan Revision E, JPL will continue fabrication process enhancement, novel device and circuit development, and noise-reduction experiments that leverage JPL's capabilities in the following areas:

1. Fabrication, measurement, and analysis of superconducting resonators;
2. Fabrication, measurement, and analysis of circuits based on superconducting tunnel junctions and related devices; and
3. Electron Paramagnetic Resonance measurements of interlayer dielectrics and interfaces.

JPL and D-Wave now seek to extend this agreement through August 2027. The amount of funding estimated previously is considered sufficient to accomplish this work through that time.

4. JPL UNIQUENESS JUSTIFICATION

The Superconducting Materials and Devices Group in MDL has considerable, long-established expertise in superconducting sensor fabrication, characterization, and application. In 2005, after visiting, and negotiating with corporate, academic, and government labs throughout the world having significant capabilities in the area of superconducting electronics, D-Wave concluded that JPL was, and remains, uniquely qualified to meet its requirements. As a result, JPL and D-Wave have collaborated to develop AQC-related fabrication since mid-2005 and have an excellent, mutually beneficial relationship.

Over the period 2008-2012, D-Wave established a fabrication capability based at the Silicon Valley Technology Center (SVTC), a commercial Research and Development (R&D) CMOS foundry. In 2013, the process was transferred to Cypress Semiconductor in Bloomington, MN. For years, D-Wave has possessed arguably the best superconductor integrated circuit process in the world. It features high throughput, high yield, and a complex vertical structure. JPL in no way competes with this industrial capability. Rather, JPL provides essential process development support. Some aspects of process development, such as introducing new materials and troubleshooting of some process-related problems require an R&D facility operating in a rapid prototyping mode. This role has been filled by NASA/JPL. D-Wave regards continued collaboration with NASA/JPL as essential to its success. In addition, JPL has specialty tools, including Molecular Beam Epitaxy (MBE) and Inductively-Coupled Plasma (ICP) Plasma Enhanced Chemical Vapor Deposition (PECVD), which are currently unavailable to D-Wave but can be assessed for potential advantages. If such a process can be demonstrated to provide critical advantages, the lengthy process of establishing it at the commercial foundry can be justified.

In collaborating with D-Wave, the JPL team has provided rapid turn-around Nb-based superconductor integrated circuit fabrication and characterization in close collaboration with D-Wave's manufacturing environment. JPL has no minimum lot size, in contrast to industrial organizations, which focus on throughput. JPL offers rapid turn-around of one-of-a-kind parts with a great deal of materials and process flexibility. It excels in developing new devices and process modules for insertion into a superconductor integrated circuit process. Specific JPL capabilities are listed in the following section. No industrial superconductor fabrication facility offers this set of capabilities.

3. JPL FACILITIES AND EQUIPMMENT

The JPL Superconducting Materials and Devices group has considerable experience in the design, fabrication, characterization and application of superconducting devices. For example, it routinely fabricates deep-sub μm Nb tunnel junctions and circuits based on them. The MDL clean room facilities include a state of the art electron beam lithography facility, 2 sub-0.25 μm deep-uv steppers, and tools for a wide range of metal and insulator deposition and etching processes. MDL also provides electrical characterization facilities covering the full range from room temperature down to a few mK. MDL has room temperature and cryogenic test facilities which are used to characterize the superconducting chips produced in this work.

Specific capabilities include:

- A superconductor circuit process with up to 4 Nb wiring layers with no minimum lot size (important for rapid turn-around on "one-off" experiments).
- This fabrication process is well-established as a low temperature process (<150 °C) that serves as a bench mark against which the higher temperature operations in D-Wave's manufacturing environment, which includes >200 °C temperatures that that can degrade junction quality/spreads, can be compared in order to understand and mitigate the effects of higher temperature.

- Deep-sub-μm device dimensions with deep-uv stepper lithography.
- Direct-write e-beam lithography for dimensions below what is possible with optical techniques.
- Low temperature deposition (< 100 °C) of a wide range of metals (including superconductors) and high quality/low loss dielectrics (e.g., using ICP PECVD).
- Epitaxial/single crystal film growth that D-Wave values for its potential in combating noise in qubits.
- A wide variety of wet chemical etches for experimentation that are not readily available in a manufacturing environment
- The ability to readily incorporate or substitute novel materials (e.g., the superconductors NbTiN, TiN_x, and Al or dielectrics such as SiN_x and a-Si).
- The ability to incorporate alternative tunnel barrier materials (e.g., AlN_x via ECR or ICP plasma nitridation) to produce more temperature resistant junctions.
- Characterization and testing from room temperature down to mK temperatures. Measurements include (a) DC electrical examination of test structures, devices, and circuits, (b) SQUID-based 1/f noise measurements from 20 mK – 4 K, (c) 20 mK broadband resonator noise measurements, and magnetic impurity characterization using Electron Paramagnetic Resonance (EPR) measurements. A specific example of importance to D-Wave is mK characterization of dielectric loss-tangents (related to two level system noise that causes decoherence in qubits).

4. BENEFITS TO NASA/JPL

Combinatorial optimization is a foundational problem of central importance to JPL and NASA, pervading mission planning, engineering design, robotics, and AI. The quantum annealing processors being developed by D-Wave can solve a wide range of combinatorial optimization problems. Future versions of the processors are expected to provide improved solution quality. Thus, this collaboration could open the door to a broad spectrum of future AQC-related work at JPL.

In addition to supporting JPL and NASA computational interests, this commercial collaboration both leverages and advances MDL superconducting sensor work in areas such as (1) Sub-μm superconducting tunnel junction fabrication in particular and superconducting circuit processing in general (e.g., sub-μm vias, high quality dielectric deposition, etching of oxides and metals, planarization, and increased circuit complexity). (2) Superconducting Quantum Interference Devices (SQUIDs). (3) Reduction of circuit noise at mK temperatures. (4) Ultralow temperature multiplexing/signal processing. This collaboration also supports key personnel and equipment and has provided significant support for MDL infrastructure.

B. OBJECTIVE

The underlying goals of this Task Plan are the development of a fabrication process for Nb-based superconductor integrated circuits and its application to build Adiabatic Quantum Computers (AQC). In this Task Plan, JPL will test device and circuit concepts, perform R&D aimed at reducing circuit noise and decoherence, improve the efficiency of heat removal from operating chips, conduct fabrication process studies, implement fabrication process improvements, devise troubleshooting tests for process control, and develop methods to evaluate process effectiveness.

C. APPROACH

This Task Plan 97-16404 builds upon the past successful tasks and will include similar kinds of work. As described in the objective, JPL will test device and circuit concepts, perform R&D aimed at reducing circuit noise and decoherence, improve the efficiency of heat removal from operating chips, conduct fabrication process studies, implement fabrication process improvements, devise troubleshooting tests for process control, and develop methods to evaluate process effectiveness.

JPL and D-Wave will be responsible for holding regular (roughly bi-weekly) meetings to decide strategy and tactics. It is anticipated that most of these meetings will be teleconferences or video conferences. These meetings include discussion and evaluation of recent results, discussion and evaluation of near-term and long-term needs, and formulation of monthly and quarterly plans for collaborative activity, including specific plans for JPL activity. JPL will be responsible for delivering on the commitments included in these plans. Typical short-term commitments include fabrication at JPL of one or several wafers, characterization of their electrical properties, and delivery of data and test chips to D-Wave as required. Alternatively, JPL performs specialized measurements on sample chips provided by D-Wave, returning reports on, and analysis of, the results obtained. Continuous communication between the parties is fundamentally important, and JPL will be responsible for providing, as needed, reports describing JPL fabrication and characterization activities, evaluation of process issues, and recommendations for future work.

Areas of past, current, and anticipated JPL activity:

- Tests of device and circuit concepts. A successful example from the existing Task is the demonstration of a novel non-dissipative qubit readout scheme that has enabled dramatic speedup of future processor chips. **(Completed)**
- Reduction of qubit and circuit noise/de-coherence. This work includes substitution of new superconductor or dielectric materials in parts of the process (or chip vertical structure)., removal of unwanted oxides on existing wiring layers, and examination of the effect of processing on interfaces and sources of magnetic flux noise. **(On-going)**
- From FY 2013 through FY 2017, this work included low-frequency 1/f noise measurements of appropriate test structures at 20 mK – 4 K. **(Completed)** Also in FY 2013, broadband resonator response measurements at 50 mK were added at JPL.

These measurements are ongoing. **(On-going)** Recently, beginning in mid-FY 2019, magnetic impurity characterization using EPR was added at JPL. **(On-going)**

- Improvement of heat transfer from operating chips by substitution of new substrates and novel interface and substrate treatments. JPL will also consult on cryogenic thermal engineering of the cooling stages used for D-Wave devices and on methods to distribute heat at sub-Kelvin temperatures. **(Completed)**
- Improving process yield through better understanding of, and controlling the effect of, oxidation temperature and small Al thickness variations on critical current density. **(Completed)**
- Fabrication process improvements, including replacement AlO_x tunnel barriers by AlN ones, allowing significantly higher process temperatures, which will allow improved interlevel dielectric layers and better device parameter control. **(Deferred)**
- Fabrication process troubleshooting via short loop runs involving JPL processing of Josephson trilayers grown by D-Wave.
- Fabrication process evaluation via analysis of data provided by D-Wave and measurements on D-Wave samples. **(On-going)**
- Support the D-Wave fabrication process via short loop runs on D-Wave-supplied wafers. **(On-going)**
  - Nb wire deposition process
    - Determine T_c and resistivity uniformity and reproducibility
  - Josephson junction trilayer deposition process
    - Determine the effect on targeting and uniformity of film stress, Al thickness, gas purity and process temperature.
    - Monitor and analyze the effect on tunnel barrier resistivity of oxygen exposure and gas composition.
    - Determine the effect on vital device parameters of thermal annealing, with and without diffusion barrier layers at key locations in the vertical structure.
    - JPL will lead the effort to develop a high-J_c (10 kA/cm^2) process at D-Wave. **(Completed)**
- Independent investigations at JPL
  - Compare techniques (wet chemical etching, ion milling, and plasma etching) for selective Nb oxide removal from wiring layers and employ Transmission Electron Microscope (TEM) cross sectional images to evaluate isotropy and selectivity. **(Completed)**
  - Develop plasma-aided growth of high-quality AlN_x tunnel barriers to allow higher processing temperatures, ultimately providing a transferrable process with adequate uniformity, junction quality. **(Deferred)**
  - SiN_x thin film deposition.
    - Evaluate stoichiometric, low temperature (<200 °C) PECVD Si_3N_4 deposition for junction hard masks and protective junction caps. Requirements include low stress, high uniformity, good adhesion to AlO_x, no resist poisoning. **(Completed)**
    - Investigate resources for obtaining sputtered or PECVD SiN_x on 200 mm wafers. Requirements include good particle control, adequate throughput.

(Completed)

- Reduce qubit body capacitance via air bridges and/or low k dielectrics.

- Collaborative process development
  - Investigations of qubit noise reduction will continue, with specific experiments to be defined based on testing by D-Wave of existing chips. These may include exploration of low temperature ICP PECVD deposition of SiO_2, SiN_x, and Si:H for interlayer dielectrics and SiN_x as a cap on wiring prior to SiO_2 deposition.JPL will develop appropriate low-frequency 1/f SQUID-based noise measurement techniques at 20 mK – 4 K and apply them to appropriate test structure designed by JPL and D-Wave. **(Completed)**
  - JPL will develop appropriate broadband resonator-based noise measurement techniques at 20 mK – 4 K and apply them to appropriate test structures designed by JPL and D-Wave. **(On-going)**
  - JPL will develop EPR measurements to investigate noise in dielectrics due to magnetic impurities and defects.
  - Experiments aimed at improving thermalization based on testing by D-Wave have been performed. **(Completed)**
- Collaborative device/circuit development **(On-going)**
  - Evaluate, as circumstances dictate, novel circuit concepts by fabricating prototype wafers at JPL, with functional testing at D-Wave. Experiments may include study of schemes to introduce X-Z coupling to qubit interactions.
- Room temperature and cryogenic testing **(On-going)**
  - Obtain statistics on Nb film T_c, ΔT_c, p, RRR, λ measurements and compare JPL and D-Wave results to refine and improve measurement techniques and analysis.
  - Develop understanding of the limits on correlating room temperature junction resistivity and low temperature critical current. Improve accuracy of extraction of I_c, R_n, V_g, ΔV_g, R_j/R_n from I-V data at 4 K and below
  - Optimize the use of process-related data to improve process yields and collaborate with D-Wave to improve databases and their analysis.

D. INFORMATION REGARDING JPL AND NASA'S RELATIONSHIP

JPL is a NASA-owned Federally Funded Research and Development Center (FFRDC) that conducts programs in Space Science and other scientific areas approved by NASA; as well as an operating division of California Institute of Technology (Caltech), staffed with regular Caltech employees. Caltech performs research at the NASA-owned JPL facility pursuant to a sponsoring agreement between NASA and Caltech.

While the facilities at JPL are government-owned, the JPL contractor, Caltech, is not an arm of the Federal Government. Its employees are not agents of the Federal Government and thus are not empowered to bind NASA to agreements with reimbursable sponsors.

Caltech operates JPL under NASA Contract 80NM0018D0004, which is administrated by Federal employees of the NASA Management Office located on-site at JPL. While Caltech is responsible for preparation of reimbursable proposals and performance of assigned tasks under the contract, agreements sending work to JPL are initiated and signed by NASA and the sponsor. Please be advised that Federal law places strict constraints on the types of work that an FFRDC, such as JPL, may perform for NASA or other sponsors.

All reimbursable work that NASA agrees to accept under Contract 80NM0018D0004 must be consistent with its terms and conditions and JPL's mission as an FFRDC as determined by the NASA Contracting Officer in accordance with Clause C-1 (b) of the 80NM0018D0004.

E. SCOPE OF WORK

JPL will actively collaborate with D-Wave Systems Inc., to (a) develop, maintain, and improve a Nb-based superconductor circuit fabrication process that meets the requirements for producing quantum computing devices designed by D-Wave, and (b) characterize and maximize functionality of the resulting circuits.

In the performance of this work, JPL will, on a best-efforts, non-interference basis:

1. Support the D-Wave fabrication process via short loop wafer fabrication runs on JPL and D-Wave-supplied wafers. **(Completed)**
2. Perform cryogenic DC electrical measurements and analysis of results on devices and other test structures fabricated at JPL or supplied by D-Wave. **(Completed)**
3. Support improvement and extension of the D-Wave foundry process via short loop fabrication of test structures and electrical characterization (cryogenic and room temperature, DC and microwave) and analysis of these structures. **(Ongoing)**
4. Investigate process and circuit performance improvements by applying unique MDL tools and processes to fabricate prototype circuits to be tested by JPL or D-Wave. **(Completed)**
5. Enable D-Wave quantum annealing processor performance improvements by applying unique MDL materials, tools, and processes to fabricate prototype circuits. **(On-going)**
6. Evaluate D-Wave's success at noise reduction in its quantum annealing processors by conducting SQUID 1/f noise measurements at 20 mK-4K and superconducting resonator measurements at mK temperatures. **(Completed)**
7. Evaluate D-Wave's success at noise reduction in its quantum annealing processors by conducting resonator noise measurements at 20 – 50 mK. **(Completed)**
8. Support efforts to reduce noise in D-Wave processors by conducting mK measurements on superconducting resonators with novel superconductors, dielectrics, and/or growth techniques. **(On-going)**
9. Exploit D-Wave's recent discovery of magnetic noise in dielectrics to enable reduction of quantum annealing processor noise by conducting Electron

Paramagnetic Resonance (EPR) measurements at room temperature on novel dielectric test samples. **(On-going)**

10. Evaluate, troubleshoot, and improve the D-Wave process by analyzing JPL and D-Wave data**. (On-going)**
11. Prepare technical progress reports as requested by D-Wave. **(On-going)**
12. Prepare a follow-on Task Plan, if requested.
13. Prepare a Final Report.
14. Participate in conferences and technical reviews held by D-Wave at JPL or at D-Wave facilities in Palo Alto, CA or Burnaby, British Columbia, Canada. **(On-going)**

F. DELIVERY SCHEDULE

JPL will deliver to D-Wave Systems:

1. Superconducting test chips for D-Wave functional testing, as requested.
2. Informal technical progress reports (JPL format), as requested.
3. One copy of a follow-on Task Plan (JPL format), if requested before **August 31, 2027**.
4. One copy of a Final Report (JPL format), due on or before **August 31, 2027**.

G. MANAGEMENT PLAN

As the JPL Task Manager, Dr. Alan Kleinsasser is responsible for the technical execution of this task, including cost, schedule, and performance. He is responsible for managing resources, coordinating the overall efforts, and accomplishing the formal deliverables identified in JPL Task Plan 82-16404. He will conduct weekly team meetings to assess team progress against the planned cost, schedule, and performance. In addition, Dr. Alan Kleinsasser must ensure that the costs remain within the allotted D-Wave funding.

H. SPECIAL PROVISIONS

1. Export Control

In the performance of this Task Plan, JPL ☐ will ☒ **will not** be required to transfer equipment, software or technical data controlled by laws and regulations of the United States, including the Export Administration Act of 1979 (50 U.S.C. App. 2401, et seq.), as amended, and the Export Control Act (22 U.S.C. 2778), as amended, and all regulations thereunder, including the International Traffic in Arms Regulations (22 C.F.R. 120-130), as amended, and Export Administration Regulations (15 C.F.R. 730-774), as amended.

The technology described in this task plan Quantum Computing Circuit Fabrication is EAR 3E003. The JPL Task Manager will ensure compliance with export requirements.

NOTE: The Task Manager will flow down the information required in this section to all task personnel

2. Human Subjects Research

☐ This work involves human subject's research. The Caltech Institutional Review Board (IRB) shall be the IRB of record for this project. Caltech IRB approval will be obtained and maintained throughout the term of this project.

☒ This work does not involve human subject's research. Use of NASA Aircraft, Unmanned Aircraft System (UAS) or Commercial Aircraft Services (CAS)

In the performance of this task it has been determined:

☐ The task **MAY** utilize the use of a NASA Aircraft, UAS or Acquisition of Commercial Air Services and will require the preparation and processing of required flight planning documentation through the NASA Management Office (NMO) and Armstrong Flight Research Center.

☒ The task **WILL NOT** utilize the use of a NASA Aircraft, UAS or Acquisition of Commercial Air Services

I. INTELLECTUAL PROPERTY

RESERVED.

No D-Wave Intellectual Property is being contemplated to be employed in the performance of the Task Plan.

J. POINTS OF CONTACT

SPONSOR	
Eric Ladizinsky	eric@dwavesys.com
Co-Founder & Chief Scientist	(408) 318-3641

NASA	
Nar Nazari	nar.r.nazari@nasa.gov
Contracting Officer	(818) 354-5619

JPL	
Alan Kleinsasser	alan.w.kleinsasser@jpl.nasa.gov
Task Manager	(818) 354-9186
Gabrielle Lee	gabrielle.d.lee@jpl.nasa.gov
Contracts Manager	(818) 354-0073

K. COST ESTIMATE (dollars expressed in whole dollars)

TO# 80NM0018F0768
Timephased Cost Estimate TP 97-16404, Revision E
(Whole Dollars Expressed)

	Legacy Actuals 1407/3001 Actuals	1804 Period Actuals thru Apr 2021	ETC FY21	ETC FY22	ETC FY23	ETC FY24	ETC FY25	ETC FY26	ETC FY27	1804 Contract Period Total	Total Lifecycle Value
JPL	$4,345,992	$948,574	$167,536	$325,000	$325,000	$325,000	$325,000	$325,000	$325,000	**$2,117,536**	**$7,412,102**
NASA Costs	$255,626	$59,180		$136,311	$136,311	$136,312	$136,312	$136,312	$136,312	**$817,870**	**$1,132,676**
Total NASA Costs	$4,601,618	$1,007,754	$167,536	$461,311	$461,311	$461,312	$461,312	$461,312	$461,312	**$2,935,406**	**$8,544,778**
Bypass											
Total MC	**$4,601,618**	**$1,007,754**	**$167,536**	**$461,311**	**$461,311**	**$461,312**	**$461,312**	**$461,312**	**$461,312**	**$2,935,406**	**$8,544,778**

Legend

JPL = JPL & Subcontracts & UFE
ONC = Other NASA Costs
Total MC = Total Management Commitment

D-Wave Systems Inc.
3033 Beta Avenue, Burnaby, BC V5G 4M9, Canada
Telephone: 604-630-1428 Fax: 604-630-1434
www.dwavesys.com

November 8, 2019

Mr. Kent Bress
Director, Aeronautics and Cross-Agency Support Division
Attn: Office of International and Interagency Relations
National Aeronautics and Space Administration
Washington DC 20546-001

Re: Amendment and extension of Reimbursable Agreement with D-Wave Systems Inc.

Dear Mr. Bress,

We are in receipt of you letter dated November 7, 2019 regarding amendments to and extension of the Reimbursable Agreement with D-Wave Systems Inc. We accept the amendments you have made to the JPL Task Plan No. 82-16404 (replaced by JPL Task Plan No. 97-16404, Revision D), the Financial Obligations for the new cost estimate and the extension of the Term of the Agreement to September 30, 2022.

We appreciate the work JPL has performed for us to date and we look forward to a continued successful relationship.

Sincerely,

DocuSigned by:
7A2EBDB5A1614CC...

Jeremy Hilton
SVP, Technology and Applications
Tel.: (604) 630-1428 x201
Email: jphilton@dwavesys.com

National Aeronautics and Space Administration

Headquarters
Washington, DC 20546-0001

November 7, 2019

Reply to Attn of: Office of International and Interagency Relations

Mr. Jeremy Hilton
Senior Vice President
of Systems
D-Wave Systems, Inc.
3033 Beta Avenue
Burnaby, British Columbia
V5C 4M9 Canada

Dear Mr. Hilton:

The purpose of this letter is to amend and extend the reimbursable Space Act Agreement between the National Aeronautics and Space Administration (NASA) and D-Wave Systems, Inc., hereinafter jointly referred to as "the Parties," for adiabatic quantum computing fabrication process development, hereinafter referred to as the "Agreement." This Agreement entered into force on June 22, 2011. The Agreement was amended and extended on July 29, 2014, and again on September 25, 2017.

I propose to amend and extend the Agreement as follows:

1) Recognition of JPL Task Plan Change:

Due to the change in the JPL Task Plan to accommodate the extension and amendment of the Agreement, the words "JPL Task Plan No. 97-16404, Revision D," are to replace all references to the JPL Task Plan in the Agreement. In addition, the Agreement's attachment of JPL Task Plan No. 82-16404, Revision C is to be replaced with JPL Task Plan No. 97-16404, Revision D, which is enclosed.

2) Financial Obligations

NASA proposes to delete Article 5, "Financial Obligations," in its entirety and replace it with the following:

"1. D-Wave Systems, Inc., agrees to reimburse NASA an estimated cost of **$8,544,778** for NASA to carry out its responsibilities under this Agreement. In no event will NASA transfer any U.S. Government funds to D-Wave Systems, Inc., under this Agreement. Payment must be made by D-Wave Systems, Inc., in advance of initiation of NASA's efforts on behalf of D-Wave Systems, Inc.

FUNDS RECEIVED TO DATE		**$ 4,800,000**
Incremental funds	Due NLT 30-Sep-2019	$ 200,000
Incremental funds	Due 3 months after SAA Amendment 4 start date	$ 300,000
Incremental funds	Due 6 months after SAA Amendment 4 start date	$ 300,000
Incremental funds	Due 9 months after SAA Amendment 4 start date	$ 300,000
Incremental funds	Due 12 months after SAA Amendment 4 start date	$ 300,000
Incremental funds	Due 15 months after SAA Amendment 4 start date	$ 300,000
Incremental funds	Due 18 months after SAA Amendment 4 start date	$ 300,000
Incremental funds	Due 21 months after SAA Amendment 4 start date	$ 300,000
Incremental funds	Due 24 months after SAA Amendment 4 start date	$ 300,000
Incremental funds	Due 27 months after SAA Amendment 4 start date	$ 300,000
Incremental funds	Due 30 months after SAA Amendment 4 start date	$ 300,000
Incremental funds	Due 33 months after SAA Amendment 4 start date	$ 300,000
Incremental funds	Due 33 months after SAA Amendment 4 start date	$ 244,778
TOTAL		**$ 8,544,778**

2. Payment shall be payable to the National Aeronautics and Space Administration through the NASA Shared Services Center (NSSC) (choose one form of payment):

   (1) U.S. Treasury FEDWIRE Deposit System, Federal Reserve Wire Network Deposit System;

   (2) Pay.gov at www.nssc.nasa.gov/customerservice (select "Pay NASA" from the Quick Links to the left of the page); or

   (3) Check sent to:

   NASA Shared Services Center
   FMD – Accounts Receivable for the Accounts of:
   Jet Propulsion Laboratory
   Building 1111

Jerry Hlass Road
Stennis Space Center, MS 39529

Payment by electronic transfer (#1 or #2, above), is strongly encouraged, and payment by check is to be used only if circumstances preclude the use of electronic transfer. All payments and other communications regarding this Agreement shall reference the Center name ("JPL"), title ("Reimbursable Space Act Agreement between NASA and D-Wave Systems for adiabatic quantum computing fabrication process development"), signature date, and number of this Agreement. NASA will provide the number of this Agreement after this amendment has been signed by both Parties.

3. NASA will not provide services or incur costs beyond the existing payment. Although NASA has made a good faith effort to accurately estimate its costs, it is understood that NASA provides no assurance that the proposed effort under this Agreement will be accomplished for the above estimated amount. Should the effort cost more than the estimate, D-Wave Systems, Inc., will be advised by NASA as soon as possible. D-Wave Systems, Inc., shall pay all costs incurred and has the option of canceling the remaining effort, or providing additional funding in order to continue the proposed effort under the revised estimate. Should this Agreement be terminated, or the effort completed at a cost less than the agreed-to estimated cost, NASA shall account for any unspent funds after completion of all effort under this Agreement, and promptly thereafter return any unspent funds to D-Wave Systems, Inc.

4. Notwithstanding any other provision of this Agreement, all activities under or pursuant to this Agreement are subject to the availability of funds, and no provision of this Agreement shall be interpreted to require obligation or payment of funds in violation of the Anti-Deficiency Act, (31 U.S.C. § 1341)."

3) Key Personnel

NASA proposes to delete the Business/Administrative Points of Contacts under Article 22, Key Personnel, and replace as follows:

"Business/Administrative Points of Contact

NASA

Nar Nazari
Contracting Officer
NASA Management Office
4800 Oak Grove Drive
Pasadena, CA 991019 U.S.A.
Telephone: (818) 354.5619
Email: nar.r.nazari@nasa.gov

D-WAVE

Jeremy Hilton
Sr. Vice President of Systems
3033 Beta Avenue
Burnaby, BC V5G 4M9
Canada
Telephone: (604) 630.1428
Email: jphilton@dwavesys.com "

4) Term of Agreement

NASA proposes to delete Article 18, "Term of Agreement", in its entirety and replace it with the following:

> "This Agreement becomes effective upon the date of the last signature below with retroactive effect to September 29, 2019, and shall remain in effect until the completion of all obligations of both Parties hereto, or September 30, 2022."

If the above terms and conditions are acceptable to D-Wave Systems, Inc., I propose that this letter, together with your affirmative reply, constitutes an amendment and extension to our Agreement that will enter into force on the date of your reply.

Sincerely,

Kent Bress
Director, Aeronautics and Cross-
Agency Support Division

Enclosures

D-Wave Systems Inc.
3033 Beta Avenue
Burnaby, BC V5G 4M9
Telephone (604) 630-1428 Facsimile (604) 630-1434
web: www.dwavesys.com

September 25, 2017

Mr. Kent Bress
Director, Aeronautics and Cross-Agency Support Division
Attn: Office of International and Interagency Relations
National Aeronautics and Space Administration
Washington DC 20546-001

Re: Amendment and extension of Reimbursable Agreement with D-Wave Systems Inc.

Dear Mr. Bress,

We are in receipt of your letter of September 25th, 2017 regarding amendments to and extension of the Reimbursable Agreement with D-Wave Systems Inc. We accept the amendments you have made to the JPL Task Plan No. 82-16404, Revision C, the Financial Obligations for the new cost estimate and the extension of the Term of the Agreement to September 29, 2019.

We appreciate the work JPL has performed for us to date and we look forward to a continued successful relationship.

Sincerely,

Warren Wall
EVP, Corporate Affairs

National Aeronautics and Space Administration

Headquarters
Washington, DC 20546-0001

September 25, 2017

Reply to Attn of: Office of International and Interagency Relations

Mr. Warren Wall
Executive Vice President
And Chief Operating Officer
D-Wave Systems, Inc.
3033 Beta Avenue
Burnaby, British Columbia
V5C 4M9 Canada

Dear Mr. Wall:

The purpose of this letter is to amend and extend the reimbursable Space Act Agreement between National Aeronautics and Space Administration (NASA) and D-Wave Systems, Inc., hereinafter jointly referred to as "the Parties," for adiabatic quantum computing fabrication process development, hereinafter referred to as the "Agreement." This Agreement entered into force on June 22, 2011. The Agreement was amended and extended on July 29, 2014 through September 30, 2017. One additional amendment took place on November 9, 2015. The Agreement is still currently set to expire on September 30, 2017.

I propose that we replace the amendment from 2015 in its entirety. Therefore, NASA proposes to amend and extend the Agreement as amended in 2014 as follows:

1) Recognition of JPL Task Plan Change:

Due to the change in the JPL Task Plan to accommodate the extension and amendment of the Agreement, the words "Revision C," are to replace the words "Revision A" after all references to "JPL Task Plan No. 82-16404" in the Agreement. In addition, the Agreement's attachment of JPL Task Plan No. 82-16404, Revision A is to be replaced with JPL Task Plan No. 82-16404, Revision C, which is enclosed.

2) Financial Obligations:

NASA proposes to delete Article 5, "Financial Obligations," in its entirety and replace it with the following:

> "1. D-Wave Systems, Inc. agrees to reimburse NASA an estimated cost of $6,107,916 for NASA to carry out its responsibilities under this Agreement. In no event will NASA transfer any U.S. Government funds to D-Wave Systems, Inc. under this

Agreement. Payment must be made by D-Wave Systems, Inc. in advance of initiation of NASA's efforts on behalf of the D-Wave Systems, Inc.

2. As a result of this Revision, the cost estimate will increase by **$1,839,285** from **$4,268,631** to **$6,107,916.**

Initial payment authorized to proceed	PAID	$4,268,631
Incremental funds	Due 04 Months after contract start date	$200,000
Incremental funds	Due 08 Months after contract start date	$200,000
Incremental funds	Due 10 Months after contract start date	$200,000
Incremental funds	Due 12 Months after contract start date	$200,000
Incremental funds	Due 14 Months after contract start date	$200,000
Incremental funds	Due 16 Months after contract start date	$200,000
Incremental funds	Due 18 Months after contract start date	$200,000
Incremental funds	Due 20 Months after contract start date	$200,000
Incremental funds	Due 24 Months after contract start date	$239,285
TOTAL:		**$6,107,916**

3. Payment shall be payable to the National Aeronautics and Space Administration through the NASA Shared Services Center (NSSC) (choose one form of payment):

(1) U.S. Treasury FEDWIRE Deposit System, Federal Reserve Wire Network Deposit System;

(2) pay.gov at www.nssc.nasa.gov/customerservice (select "Pay NASA" from the Quick Links to the left of the page); or

(3) check. A check should be payable to NASA and sent to:

NASA Shared Services Center
FMD – Accounts Receivable For the Accounts of:
Jet Propulsion Laboratory
Building 1111,
Jerry Hlass Rd.,
Stennis Space Center, MS 39529

Payment by electronic transfer (#1 or #2, above), is strongly encouraged, and payment by check is to be used only if circumstances preclude the use of electronic transfer. All payments and other communications regarding this Agreement shall reference the Center name, title, date, and number of this Agreement.

4. NASA will not provide services or incur costs beyond the existing payment. Although NASA has made a good faith effort to accurately estimate its costs, it is understood that NASA provides no assurance that the proposed effort under this Agreement will be accomplished for the above estimated amount. Should the effort cost more than the estimate, Partner will be advised by NASA as soon as possible. Partner shall pay all costs incurred and has the option of canceling the remaining effort, or providing additional funding in order to continue the proposed effort under the revised estimate. Should this Agreement be terminated, or the effort completed at a cost less than the agreed-to estimated cost, NASA shall account for any unspent funds after completion of all effort under this Agreement, and promptly thereafter return any unspent funds to Partner.

5. Notwithstanding any other provision of this Agreement, all activities under or pursuant to this Agreement are subject to the availability of funds, and no provision of this Agreement shall be interpreted to require obligation or payment of funds in violation of the Anti-Deficiency Act, (31 U.S.C. § 1341)."

3) Term of Agreement:

NASA proposes to delete Article 18, "Term of Agreement", in its entirety and replace it with the following:

"This Agreement becomes effective upon the date of the last signature below and shall remain in effect until the completion of all obligations of both Parties hereto, or September 29, 2019, whichever comes first."

If the above terms and conditions are acceptable to D-Wave Systems, Inc., I propose that this letter, together with your affirmative reply, constitutes an amendment and extension to our Agreement that will enter into force on the date of your reply.

Sincerely,

Kent Bress
Director, Aeronautics and Cross-
Agency Support Division

Enclosures

D-Wave Systems Inc.
3033 Beta Avenue
Burnaby, BC V5C 6G9
Telephone (604) 630-1428 Facsimile (604) 630-1434
web: www.dwavesys.com

July 31, 2014

Mr. Kent Bress
Director, Aeronautics and Cross-Agency Support Division
National Aeronautics and Space Administration
Washington DC 20546-0001

Re: Reimbursable Agreement with D-Wave Systems Inc.

Dear Mr. Bress,

We are in receipt of your letter of July 29, 2014 regarding an amendment to the Reimbursable Agreement with D-Wave Systems Inc. We accept the amendments you have made to the JPL Task Plan, the Financial Obligations for the new cost estimate and the extension of the Term of the Agreement to September 30, 2017.

We appreciate the work JPL has performed for us to date and we look forward to a continued successful relationship.

Sincerely,

W Wall

Warren Wall
EVP, Chief Operating Officer

National Aeronautics and Space Administration

Headquarters
Washington, DC 20546-0001

July 29, 2014

Reply to Attn of: Office of International and Interagency Relations

Mr. Warren Wall
Executive Vice President
And Chief Operating Officer
D-Wave Systems, Inc.
3033 Beta Avenue
Burnaby, British Columbia
V5C 4M9 Canada

Dear Mr. Wall:

The purpose of this letter is to amend and extend the reimbursable Space Act Agreement between National Aeronautics and Space Administration (NASA) and D-Wave Systems, Inc., hereinafter jointly referred to as "the Parties," for adiabatic quantum computing fabrication process development, hereinafter referred to as the "Agreement." This Agreement entered into force on June 22, 2011, and is currently set to expire on September 30, 2014.

I propose that we amend and extend the Agreement as follows:

1) Recognition of JPL Task Plan Change:

Due to the change in the JPL Task Plan to accommodate the extension of the Agreement, the words "Revision A," are to be inserted after all references to "JPL Task Plan No. 82-16404" in the Agreement. In addition, the Agreement's attachment of JPL Task Plan No. 82-16404 is to be replaced with JPL Task Plan No. 82-16404, Revision A, which is enclosed.

2) Financial Obligations:

a) Due to the amendment and extension of this Agreement, the total cost estimate is increased by $1,022,437. As a result, the estimated cost of "**$2,556,093**," shown in Article 6, paragraph 2, of the Agreement, is to be replaced with the new estimated cost of "**$3,578,530**." The payment schedule provided on page 3 of the Agreement is to be deleted in its entirety, and replaced with the revised payment schedule below:

Transaction	Date	Increment	Subtotal
Initial payment authorized to proceed	Paid June 24, 2011	$200,000	
Incremental funds	Paid August 26, 2011	$200,000	
Incremental funds	Paid December 01, 2011	$139,746	
Transfer from previous task NMO715967	Transferred Q1 FY 2012	$60,254	
Incremental funds	Paid April 20, 2012	$100,000	
Incremental funds	Paid July 2. 2012	$200,000	
Incremental funds	Paid November 27, 2012	$200,000	
Incremental funds	Paid March 5, 2013	$200,000	
Incremental funds	Paid June 7, 2013	$100,000	
Incremental funds	Paid August 26, 2013	$200,000	
Incremental funds	Paid November 25, 2013	$200,000	
Incremental funds	Due June 1, 2014	$200,000	
Incremental funds	Due September 1, 2014	$200,000	
Incremental funds	Due December 1, 2014	$200,000	
Incremental funds	Due March 1, 2015	$156,093	$2,556,093
Revision A initial funds	Due March 1, 2015	$43,907	
Incremental funds	Due June 1, 2015	$200,000	
Incremental funds	Due September 1, 2015	$200,000	
Incremental funds	Due December 1, 2015	$200,000	
Incremental funds	Due March 1, 2016	$200,000	
Incremental funds	Due June 1, 2016	$178,530	$1,022,437
Total		$3,578,530	$3,578,530

b) NASA proposes to replace paragraphs 4 through 6 of Article 6 with the following new paragraphs 4 - 6:

"4. Payment shall be payable to "the National Aeronautics and Space Administration (NASA)" through the NASA Shared Services Center (NSSC) via: [1] electronically submitting funds through the Pay.gov system (https://pay.gov/paygov/), a secure, government-wide, internet collection portal; or [2] check. Payment by electronic transfer is strongly encouraged, and payment by check is to be used only if circumstances preclude the use of electronic transfer. All payments and other communications regarding this Agreement shall reference the NASA field center ("NASA/Jet Propulsion Laboratory (JPL)"), title of this agreement ("Reimbursable Agreement with D-Wave Systems Inc."), date, and number of this Agreement ("82-16404, RevA"). If you elect to send your check to NSSC, include a cover letter indicating funds are to be applied to NASA Space Act Agreement 82-16404, RevA, and mail to the following address:

NASA Shared Service Center (NSSC)-FMD Accounts Receivable
Attention: Mr. Dawnyel Stuart, for the accounts of NASA/JPL
Building 1111, C Road
Stennis Space Center, MS 39529

5. Whichever method D-Wave Systems, Inc. uses to submit payment, D-Wave Systems, Inc. will notify the JPL Contract Administrator, Ms. Helen L. Tanabe, of the payment by sending a copy of the check or electronic confirmation of NSSC receipt via email to her at: helen.l.tanabe@jpl.nasa.gov for tracking purposes. Should you choose the Pay.gov option, instructions are included.

6. Although NASA has made a good faith effort to accurately estimate its costs, it is understood that NASA provides no assurance that the proposed effort under this Agreement will be accomplished for the above estimated amount. Should the effort cost more than estimated, D-Wave Systems, Inc. will be advised by NASA as soon as possible. D-Wave Systems, Inc. shall pay all costs incurred and have the option of canceling the remaining effort, or providing additional funding in order to continue the proposed effort under the revised estimate. Should the Agreement be terminated, or the effort completed and cost less than the agreed to estimated cost, NASA shall account for any unspent funds after completion of all effort under this Agreement, and promptly thereafter, return any unspent funds to D-Wave Systems, Inc."

3) Term of Agreement:

NASA proposes to replace the expiration date of "**September 30, 2014**" in Article 18 with the new date of "**September 30, 2017.**"

If the above terms and conditions are acceptable to D-Wave Systems, Inc., I propose that this letter, together with your affirmative reply, constitutes an amendment to our Agreement that will enter into force on the date of your reply.

Sincerely,

Kent Bress
Director, Aeronautics and Cross-
Agency Support Division

Enclosures

ADIABATIC QUANTUM COMPUTING FABRICATION PROCESS DEVELOPMENT

to

D-Wave Systems Inc.
3033 Beta Avenue
Burnaby, BC, V5C 4M9 Canada

JPL Task Plan No. 82-16404. Revision A

JET PROPULSION LABORATORY
California Institute of Technology
Pasadena, California 91109

Revision Statement

This Task Plan No. 82-16404 Revision A extends the contract by 3 years through September 30, 2017 and increases the contract value by $1,022,437.

As a result the total cost estimate will increase by $1,022,437 from $2,556,093 to $3,578,530.

Note: The Task Plan is restated in full text. The Revision A will replace and supersede Basic Task Plan. All changes in the text are indicated with vertical change bars in the right margin.

TABLE OF CONTENTS

ARTICLE 2. PURPOSE AND AGENCY COMMITMENT

A. INTRODUCTION

1. BACKGROUND

Advanced computer technology is critical to supporting JPL mission objectives. In particular, combinatorial optimization represents a problem class of central importance that pervades mission planning, engineering design, robotics and artificial intelligence. D-Wave Systems Inc. (hereinafter referred to as "D-Wave"), is developing Adiabatic Quantum Computing (AQC) as an approach to solving complex optimization problems by encoding data in arrays of Superconducting Quantum Interference Devices (SQUIDs) that act as quantum bits (qubits). The system remains in its ground state while adiabatically evolving from a simple, known configuration to a final configuration that provides the answer to the computational problem of interest. D-Wave has made numerous demonstrations of prototype AQC processors, which are projected to outperform conventional supercomputers by a wide margin within a handful of years.

JPL and D-Wave began a highly successful collaboration in 2005 under JPL Task Plan 82-10225, "Nb Quantum Computing" (Task Order NMO715801). The collaboration expanded in 2007 under JPL Task Plan 82-11375, "Nb Quantum Computing Circuit Fabrication" (Task Order NMO715967). Task Plan 82-11375 ended on June 26, 2011. Both D-Wave and JPL continued their successful collaboration through September 30, 2014 under this follow-on Task Plan, 82-16404. The nature and scope of the follow-on work described here are very similar to the work involved in Task Plan 82-11375.

Beginning in 2005, the JPL Microdevices Lab (MDL) fabricated prototype circuits and processor chips for D-Wave, beginning with single devices and individual qubits. By late 2007, D-Wave was solving benchmark problems using a 28 qubit processor fabricated at JPL, enabling a critical experimental examination of the AQC approach and the beginning of scaling studies of computational power with the number of qubits in the array. In parallel, D-Wave and JPL developed classical superconducting circuitry to control the quantum circuits. In these collaborative efforts, JPL was the sole source of quantum hardware for D-Wave, handling process development, fabrication, and initial characterization while D-Wave handled circuit designs and functional testing.

D-Wave and JPL have always viewed this work as ongoing. The aforementioned successes in this Task led D-Wave and JPL to seek to extend their collaboration through FY 2017. The changes in scope are relatively minor, as most of the planned new work is an extension of existing plans.

By 2008, in anticipation of eventual commercial success and with technical support from JPL, D-Wave developed its own chip manufacturing capability. For the past several years, D-Wave has produced complex superconducting quantum processor chips with a

distributed process based on SVTC, a commercial Complementary Metal Oxide Semiconductor (CMOS) circuit foundry in San Jose, CA. In 2013, the D-Wave process was transferred to Cypress Semiconductor in Bloomington, MN. The availability of this process, arguably the most advanced superconductor process in the world, allows D-Wave to fabricate and yield 512-qubit chips containing over 30,000 Josephson junctions. These are the most complex superconducting chips currently being produced anywhere. However, D-Wave had to continue to advance its process in order to meet new goals. These goals included demonstrating functional 512-qubit processors, each containing over 50,000 Josephson junctions, by the spring of 2012 and 2048 qubit processors, each containing over 300,000 junctions, in 2014-2015. Achieving these and future goals requires continuous process improvement. To that end, JPL remains an essential partner of D-Wave.

In any modern CMOS foundry, troubleshooting typical fabrication-related problems and introducing new materials and processes is costly and time-consuming. Fabricating superconductor circuits in such a facility introduces additional difficulties, as some essential materials and processes are non-standard. Although the benefits of operating a non-standard process in such a facility outweigh the costs, D-Wave's experience has taught that running, maintaining, and advancing its superconductor process requires close collaboration with an R&D facility operating in a rapid prototyping mode. This role has been filled by JPL, and D-Wave regards continued collaboration with JPL as essential to its success. This Task Plan defines for JPL a continuing R&D role that emphasizes support for D-Wave's manufacturing process development, rapid prototyping of advanced designs, new circuit approaches, and fundamental physical investigations.

During the first two years of this Task, much was accomplished:

- Process development
  - JPL diagnostic measurements and analysis enabled D-Wave to mitigate several problems related to excessive heating of wafers containing Josephson junctions during the fabrication process.
  - JPL has led experimental work that has enabled D-Wave to establish a high-critical current density (J_c = 10 kA/cm^2) process. This will enable D-Wave to add a second junction layer in its process. It will also allow D-Wave to supply wafers for classical single flux quantum computing circuits for anticipated government projects.
  - JPL made significant advances in implementing and understanding the use of room temperature device resistance measurements as a proxy for cryogenic critical supercurrent measurements at millikelvin temperatures. In particular, JPL developed corrections for parasitic device resistance at room temperature that allow the measurements to be applied to high-J_c wafers. This resulted in a joint publication [Alan W. Kleinsasser, Talso Chui, Bruce Bumble, and Eric G. Ladizinsky, "Critical Current Density and Temperature Dependence

of Nb-Al Oxide-Nb Junction Resistance and Implications for Room Temperature Characterization", IEEE Trans. Appl. Supercond. **23** (3), 1100405 (2013)].

- D-Wave process transfer
  - D-Wave's circuit manufacturing process was carried out at SVTC in San Jose, CA from 2008 – 2012. In September 2012, SVTC suddenly announced that it would cease operations by the end of the year. D-Wave transferred its process to Cypress Semiconductor in Bloomington, MN in early 2013. The new process is fully operational and has yielded the first functional 512-qubit quantum annealing chips. JPL provided much essential technical support during the transfer and in bringing up the process at Cypress. For example, JPL measurements and analysis were essential in establishing a new Nb deposition in a Cypress Endura cluster deposition system and in re-establishing, and advancing, the D-Wave trilayer Josephson junction growth process in its relocated Axcela cluster tool (e.g., studying feasibility of tunnel barrier growth in the ICP chamber for better uniformity and reproducibility and mapping out R_nA vs. exposure and junction quality vs. R_nA).

- JPL noise measurements (in anticipation of ongoing noise reduction experiments at JPL)
  - 1/f noise measurements
    - In FY 2013, JPL built a cryogenic probe set up SQUID 1/f noise measurements at 4 K. JPL is working with D-Wave to establish the relationship between these results and more cumbersome macroscopic resonant tunneling measurements at D-Wave.
    - Beginning in FY 2014, JPL is currently in the process of extending its SQUID measurements to mK temperatures.
    - Designed new test chips with D-Wave for experiments involving fabrication at both JPL and D-Wave.
  - Broadband noise measurements
    - In FY 2013, JPL demonstrated resonator-based broadband noise measurements at mK temperatures on D-Wave chips.
    - Designed new test chips with D-Wave for experiments involving fabrication at both JPL and D-Wave. Starting experiments with D-Wave chips.

2. JPL UNIQUENESS JUSTIFICATION

The Superconducting Materials and Devices Group in MDL has considerable, long-established expertise in the area of superconducting sensor fabrication, characterization, and application. In 2005, after visiting, and negotiating with corporate, academic, and government labs throughout the world having significant capabilities in the area of superconducting electronics, D-Wave concluded that JPL was, and is, uniquely qualified

to meet its requirements. As a result, JPL and D-Wave have collaborated to develop AQC-related fabrication since mid-2005 and have an excellent, mutually beneficial relationship.

Over the period 2008-2012, D-Wave has established a fabrication capability based at the Silicon Valley Technology Center (SVTC), a commercial Research and Development (R&D) CMOS foundry. In 2013, the process was transferred to Cypress Semiconductor in Bloomington, MN. D-Wave boasts what is arguably the best superconductor process in the world. It features high throughput, high yield, and a complex vertical structure. JPL in no way competes with this industrial facility. Rather, JPL provides essential process development support. Some aspects of process development (e.g., introducing new materials) and troubleshooting of some process-related problems require an R&D facility operating in a rapid prototyping mode. This role has been filled by NASA/JPL, and D-Wave regards continued collaboration with NASA/JPL as essential to its success. In addition, JPL has specialty tools, including Molecular Beam Epitaxy (MBE) and Inductively-Coupled Plasma (ICP) Plasma Enhanced Chemical Vapor Deposition (PECVD), which are currently unavailable at SVTC but can be assessed for potential advantages. If such a process can be demonstrated to provide critical advantages, the lengthy process of establishing it at the commercial foundry can be justified.

In collaborating with D-Wave, the JPL team has provided rapid turn-around Nb-based superconductor integrated circuit fabrication and characterization in close collaboration with D-Wave's manufacturing environment. JPL has no minimum lot size, in stark contrast to industrial organizations, which focus on throughput. JPL offers rapid turn-around of one-of-a-kind parts with a great deal of materials and process flexibility. It excels in developing new devices and process modules for insertion into a superconductor integrated circuit process. Specific JPL capabilities are listed in the following section. No industrial superconductor fabrication facility offers this set of capabilities.

3. JPL FACILITIES AND EQUIPMMENT

The JPL Superconducting Materials and Devices group has considerable experience in the design, fabrication, characterization and application of superconducting devices, routinely fabricating deep-sub μm Nb tunnel junctions, and circuits based on them. The MDL clean room facilities include a state of the art electron beam lithography facility, a sub-0.25 μm deep-uv stepper, and deposition and processing equipment for a wide range of metal and insulator deposition and etching processes. MDL also provides dc and radio frequency, electrical characterization facilities covering the full range from room temperature down to a few mK. In particular, MDL has an automated room temperature probe station and numerous cryogenic test facilities which are used to characterize the superconducting chips produced in this work.

Specific capabilities include:

- A Nb-based superconductor circuit process with up to 4 Nb wiring layers and no minimum lot size (important for rapid turn-around on "one-off" experiments).
- A well-established, low temperature fabrication process (<100 °C) that serves as a bench mark process against which the higher temperature processes in D-Wave's manufacturing environment (which includes >200 °C temperatures that that can degrade junction quality/spreads) can be compared (to understand and mitigate the effects of higher temperature)
- Deep-sub-μm device dimensions with deep-uv lithography.
- Direct-write e-beam lithography for dimensions below what is possible with optical techniques.
- Low temperature deposition (< 100 °C) of a wide range of high quality/low loss dielectrics (e.g., using ICP PECVD).
- Epitaxial/single crystal film growth that D-Wave values for its potential in combating noise in qubits.
- A wide variety of wet chemical etches for experimentation that are not readily available in a manufacturing environment
- The ability to readily incorporate or substitute novel materials (e.g., the superconductors NbTiN, TiN_x, and Al or dielectrics such as SiN_x and a-Si).
- The ability to incorporate alternative tunnel barrier materials (e.g., AlN_x via ECR or ICP plasma nitridation) to produce more temperature resistant junctions.
- Characterization and testing from room temperature down to mK temperatures. Measurements include DC electrical examination of test structures, devices, and circuits, SQUID-based 1/f noise measurements from 20 mK – 4 K, and 20 mK broadband resonator noise measurements. A specific example of importance to D-Wave is mK characterization of dielectric loss-tangents (related to two level system noise that causes decoherence in qubits).

4. BENEFITS TO NASA/JPL

Combinatorial optimization is a foundational problem of central importance to JPL and NASA, pervading mission planning, engineering design, robotics, and AI. The AQC processors being developed by D-Wave can solve a wide range of combinatorial optimization problems. Future versions of the processors are expected to provide dramatic speed-up and improved solution quality. Thus, this collaboration opens the door to a broad spectrum of future AQC-related work at JPL.

In addition to supporting JPL and NASA interests in combinatorial optimization and quantum computing, this commercial collaboration both leverages and advances MDL superconducting sensor work in areas such as (1) Sub-μm superconducting tunnel junction fabrication in particular and superconducting circuit processing in general (e.g., sub-μm vias, high quality dielectric deposition, etching of oxides and metals, planarization, and increased circuit complexity). (2) Superconducting Quantum Interference Devices (SQUIDs). (3) Reduction of circuit noise at mK temperatures. (4) Ultralow temperature multiplexing/signal processing. This collaboration also supports

key personnel and equipment and has provided significant support for MDL infrastructure

B. OBJECTIVE

The underlying goals of this Task Plan are the development of a fabrication process for Nb-based superconductor integrated circuits and its application to build Adiabatic Quantum Computers (AQC). In this Task Plan, JPL will test device and circuit concepts, perform R&D aimed at reducing circuit noise and decoherence, improve the efficiency of heat removal from operating chips, conduct fabrication process studies, implement fabrication process improvements, devise troubleshooting tests for process control, and develop methods to evaluate process effectiveness.

C. APPROACH

This Task Plan 82-16404 builds upon the past successful tasks and will include similar kinds of work. As described in the objective, JPL will test device and circuit concepts, perform R&D aimed at reducing circuit noise and decoherence, improve the efficiency of heat removal from operating chips, conduct fabrication process studies, implement fabrication process improvements, devise troubleshooting tests for process control, and develop methods to evaluate process effectiveness.

JPL and D-Wave will be responsible for holding regular (bi-weekly to monthly) meetings to decide strategy and tactics. These meetings include discussion and evaluation of recent results, discussion and evaluation of near-term and long-term needs, and formulation of monthly and quarterly plans for collaborative activity, including specific plans for JPL activity. JPL will be responsible for delivering on the commitments included in these plans. As with the existing Task Plan, typical short-term commitments include fabrication at JPL of one or several wafers, characterization of their electrical properties, and delivery of test chips to D-Wave as required. Continuous communication between the parties is fundamentally important, and JPL will be responsible for providing, as needed, reports describing JPL fabrication and characterization activities, evaluation of process issues, and recommendations for future work.

Broad areas of anticipated JPL activity include:

- Tests of device and circuit concepts. A successful example from the existing Task is the demonstration of a novel non-dissipative qubit readout scheme that has enabled dramatic speedup of future processor chips.
- Reduction of qubit and circuit noise/de-coherence. This work includes substitution of new superconductor or dielectric materials in parts of the process (or chip vertical structure), removal of unwanted oxides on existing wiring layers, and examination of the effect of processing on interfaces and sources of

magnetic flux noise. Beginning in FY 2013, this work will include broadband and low-frequency 1/f noise measurements of appropriate test structures at 20 mK – 4 K at JPL.

- Improvement of heat transfer from operating chips by substitution of new substrates and novel interface and substrate treatments. JPL will also consult on cryogenic thermal engineering of the cooling stages used for D-Wave devices and on methods to distribute heat at sub-Kelvin temperatures.
- Improving process yield through better understanding of, and controlling the effect of, oxidation temperature and small Al thickness variations on critical current density.
- Fabrication process improvements, including replacement AlO_x tunnel barriers by AlN ones, allowing significantly higher process temperatures, which will allow improved interlevel dielectric layers and better device parameter control.
- Fabrication process troubleshooting via short loop runs involving JPL processing of Josephson trilayers grown by D-Wave.
- Fabrication process evaluation via analysis of data provided by D-Wave and measurements on D-Wave samples.

The following specific activities are planned for the first three years:

- Support the D-Wave fabrication process via short loop runs on sponsor-supplied wafers.
  - Nb wire deposition process
    - Determine T_c and resistivity uniformity and reproducibility
  - Josephson junction trilayer deposition process
    - Determine the effect on targeting and uniformity of film stress, Al thickness, gas purity and process temperature.
    - Monitor and analyze the effect on tunnel barrier resistivity of oxygen exposure and gas composition.
    - Determine the effect on vital device parameters of thermal annealing, with and without diffusion barrier layers at key locations in the vertical structure.
    - JPL will lead the effort to develop a high-J_c (10 kA/cm^2) process at D-Wave.
- Independent investigations at JPL
  - Compare techniques (wet chemical etching, ion milling, and plasma etching) for selective Nb oxide removal from wiring layers and employ Transmission Electron Microscope (TEM) cross sectional images to evaluate isotropy and selectivity.
  - Develop plasma-aided growth of high-quality AlN_x tunnel barriers to allow higher processing temperatures, ultimately providing a transferrable process with adequate uniformity, junction quality
  - SiN_x thin film deposition
    - Evaluate stoichiometric, low temperature (<200 °C) PECVD Si_3N_4 deposition for junction hard masks and protective junction caps.

Requirements include low stress, high uniformity, good adhesion to AlO_x, no resist poisoning.
    - Investigate resources for obtaining sputtered or PECVD SiN_x on 200 mm wafers. Requirements include good particle control, adequate throughput.
  - Reduce qubit body capacitance via air bridges and/or low k dielectrics.
- Collaborative process development
  - Investigations of qubit noise reduction will continue, with specific experiments to be defined based on testing by D-Wave of existing chips. These may include exploration of low temperature ICP PECVD deposition of SiO_2, SiN_x, and Si:H for interlayer dielectrics and SiN_x as a cap on wiring prior to SiO_2 deposition.
  - JPL will develop appropriate broadband resonator-based and low-frequency 1/f SQUID-based noise measurement techniques at 20 mK – 4 K and apply them to appropriate test structure designed by JPL and D-Wave.
  - Experiments aimed at improving thermalization experiments will continue, with specific experiments to be defined based on testing by D-Wave of existing chips. These may include sapphire substrates, new bonding materials, and backside coatings.
- Collaborative device/circuit development
  - Evaluate, as circumstances dictate, novel circuit concepts by fabricating prototype wafers at JPL, with functional testing at D-Wave. Experiments may include study of schemes to introduce X-Z coupling to qubit interactions.
- Room temperature and cryogenic testing
  - Obtain statistics on Nb film T_c, ΔT_c, p, RRR, λ measurements and compare JPL and D-Wave results to refine and improve measurement techniques and analysis.
  - Develop understanding of the limits on correlating room temperature junction resistivity and low temperature critical current. Improve accuracy of extraction of I_c, R_n, V_g, ΔV_g, R_j/R_n from I-V data at 4 K and below
  - Optimize the use of process-related data to improve process yields and collaborate with D-Wave to improve databases and their analysis.

D. INFORMATION REGARDING JPL AND NASA'S RELATIONSHIP

The Jet Propulsion Laboratory (JPL) is a government-owned contractor operated Federally Funded Research and Development Center (FFRDC) that conducts programs in Space Science and other scientific areas approved by its sponsor, NASA. JPL is operated for NASA by the California Institute of Technology (Caltech), which is a private educational institution.

Neither JPL nor Caltech is an arm of the Federal Government nor are any of their employee's agents of the Federal Government empowered to bind NASA to agreements with reimbursable sponsors.

Caltech operates JPL under NASA Contract **NNN12AA01C,** which is administrated by Federal employees of the NASA Management Office located on-site at JPL. While Caltech is responsible for preparation of reimbursable proposals and performance of assigned tasks under the contract, agreements sending work to JPL are executed between Contracting Officers of the NASA Management Office, and the sponsor. Please be advised that Federal law places strict constraints on the types of work that an FFRDC, such as JPL, may perform for NASA or other sponsors.

All reimbursable work that NASA agrees to accept under **NNN12AA01C** must be consistent with its terms and conditions and JPL's mission as an FFRDC as determined by the NASA Contracting Officer in accordance with Clause C-1 (b) of the **NNN12AA01C.**

E. SCOPE OF WORK

JPL will actively collaborate with D-Wave Systems Inc., to (a) develop, maintain, and improve a Nb-based superconductor circuit fabrication process that meets the requirements for producing quantum computing devices designed by the sponsor, and (b) characterize and maximize functionality of the resulting circuits.

In the performance of this work, JPL will, on a best-efforts, non-interference basis:

1. Support the D-Wave fabrication process via short loop wafer fabrication runs on sponsor-supplied wafers.
2. Perform cryogenic DC electrical measurements and analysis of results on devices and other test structures fabricated at JPL or supplied by D-Wave.
3. Investigate process and circuit performance improvements by applying unique MDL tools and processes to fabricate prototype circuits to be tested by JPL or D-Wave.
4. Evaluate, troubleshoot, and improve the D-Wave process by analyzing JPL and customer data.
5. Prepare technical progress reports as requested by D-Wave.
6. Prepare a follow-on Task Plan, if requested.
7. Prepare a Final Report.

Additional Scope of Revision A:

8. **Perform forward-looking investigations into noise reduction in D-Wave processors based on SQUID i/F noise measurements at 20 mK -4K and superconducting resonator measurements at mK temperatures.**

9. **Attend technical review in Burnaby British Columba, Canada.**

ARTICLE 3. RESPONSIBILITIES

A. MANAGEMENT PLAN

As the JPL Task Manager, Dr. Alan Kleinsasser is responsible for the technical execution of this task, including cost, schedule, and performance. He is responsible for managing resources, coordinating the overall efforts, and accomplishing the formal deliverables identified in JPL Task Plan 82-16404. He will conduct weekly team meetings to assess team progress against the planned cost, schedule, and performance. In addition, Dr. Alan Kleinsasser must ensure that the costs remain within the allotted sponsor funding.

B. EXPORT COMPLIANCE

The technology described in this task plan Quantum Computing Circuit Fabrication is EAR 3E003. The JPL Task Manager will ensure compliance with export requirements.

C. HUMAN SUBJECTS RESEARCH

☐ **This work involves human subjects research. The Caltech Institutional Review Board (IRB) shall be the IRB of record for this project. Caltech IRB approval will be obtained and maintained throughout the term of this project.**

☒ **This work does not involve human subjects research.**

ARTICLE 4. SCHEDULE AND MILESTONES

A. DELIVERY SCHEDULE

JPL will deliver to D-Wave Systems:

1. Superconducting test chips for D-Wave functional testing, as requested.
2. ~~Informal technical progress reports (JPL format), as requested~~. **Deleted**
3. One copy of a follow-on Task Plan (JPL format), if requested before **August 30, 2017.**

4. One copy of a Final Report (JPL format), due on or before **September 30, 2017**.

ARTICLE 5. FINANCIAL OBLIGATIONS

TO# NNN13R220T
Timephased Cost Estimate
(Whole Dollars Expressed)

	Legacy Actuals (1407/3001)	1201 Period Actuals thru Sept FY13	FY14	FY15	FY16	FY17	1201 Contract Period Total	Total Lifecycle Value
JPL	$673,861	$518,754	$1,279,959	$313,435	**$322,641**	**$325,045**	**$2,759,834**	**$3,433,695**
NASA Costs	$24,417		$59,102	$19,996	**$20,583**	**$20,737**	**$120,418**	**$144,835**
Total NASA Costs	$698,278	$518,754	$1,339,061	$333,431	**$343,224**	**$345,782**	**$2,880,252**	**$3,578,530**
Bypass								
Total MC	**$698,278**	**$518,754**	**$1,339,061**	**$333,431**	**$343,224**	**$345,782**	**$2,880,252**	**$3,578,530**

Legend

JPL = JPL & Subcontracts & UFE
ONC = Other NASA Costs
Total MC = Total Management Commitment

A. COST ESTIMATE (dollars expressed in whole dollars)
Cost by Contractual/Programmatic

COST ESTIMATE (expressed in whole dollars)

Cost by Fiscal Year

	Revision A			
	FY 2015	**FY 2016**	**FY 2017**	**Task Plan Total**
1. Workhours				
JPL Hours	1437	1437	1437	4311
Cat A Hours	0	0	0 0	0
2. Total Direct Compensation (includes Employee Benefits)	$146,338	$151,694	$158,064	$456,096
3. Travel	$2,808	$8,032	$2,988	$13,828
4. JPL Services	$22,000	$22,000	$22,000	$66,000
5. Procurements				
Chargebacks	$8,851	$8,851	$8,851	$26,553
Subcontracts	$0	$0	$0	$0
Procurement RSA	$0	$0	$0	$0
Purchases Orders	$36,000	$36,000	$36,000	$108,000
Procurement IA	$0	$0	$0	$0
Caltech Transfers	$0	$0	$0	$0
6. Multi-Program Support	$16,741	$15,936	$16,055	$48,732
7. Total Direct Costs	**$232,738**	**$242,513**	**$243,958**	**$719,209**
8. Allocated Direct Charge	$80,697	$80,128	$81,087	$241,912
9. Total JPL Costs	**$313,435**	**$322,641**	**$325,045**	**$961,122**
10. NASA Costs	$19,996	$20,583	$20,737	$61,316
11. Total Estimated Cost	**$333,431**	**$343,224**	**$345,782**	**$1,022,437**

1. Labor

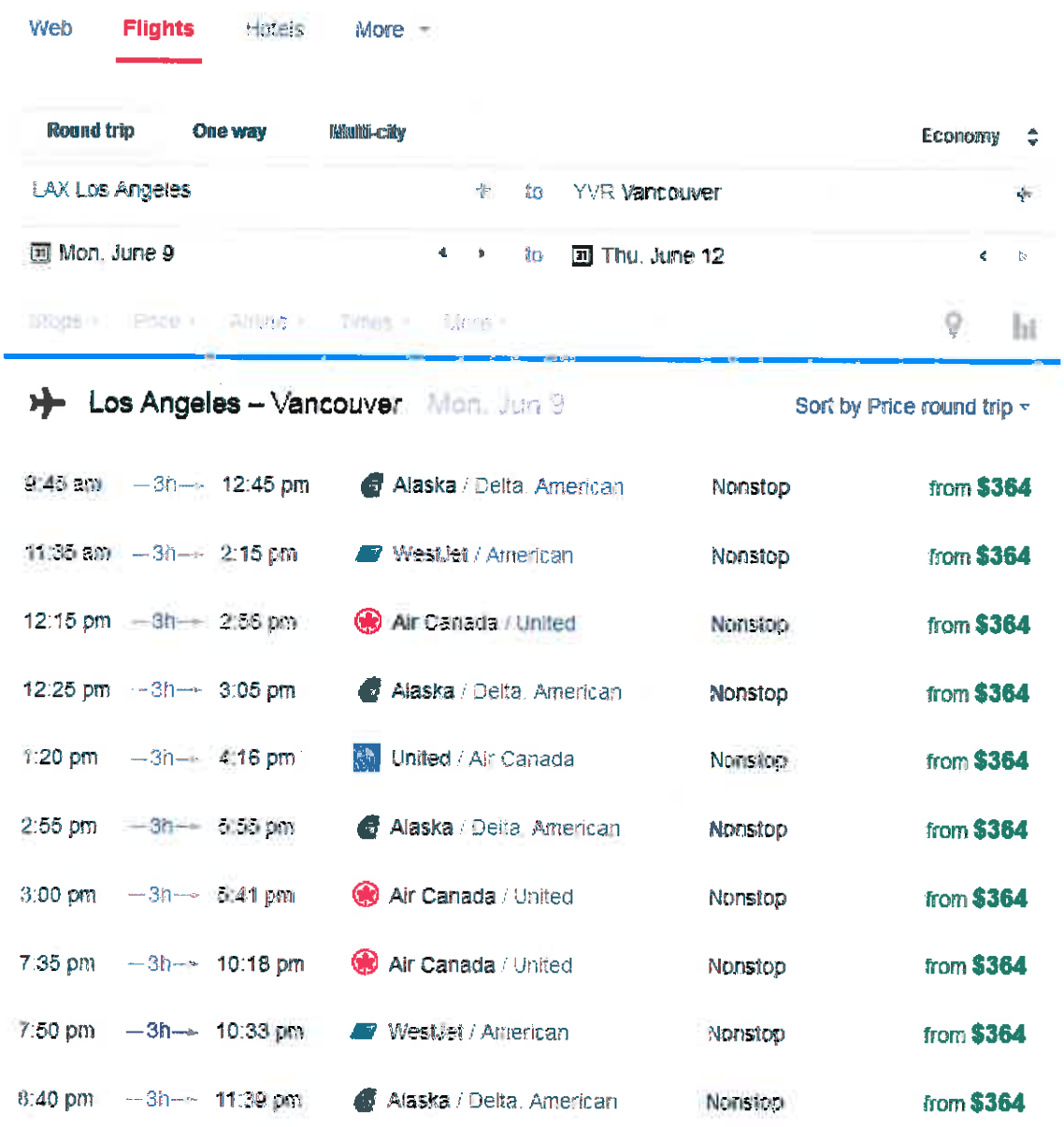
The labor estimate is a level of effort estimated by the proposal manager. The period of performance for this program starts October 2014 (FY15) and continuing through September 2016 (FY17).

	Fiscal Year (Hours)			
Labor Category	**FY 15**	**FY 16**	**FY 17**	**Total**
Engineering 4	1,343	1,343	1,343	4,029
GS-Mgmt Time	64	64	64	193
STA	30	30	30	89
Total	**1,437**	**1,437**	**1,437**	**4,311**

2. Travel

Travel was priced using JPL FY14-2 published airfare and per diem rates. The Domestic-All Other rate was used for travel to AZ, MN, and NC. Airfare to Vancouver, Canada, was priced using flights.google.com and the per diem rate was taken from the GSA website.

FY	Destination	Reason for trip	No. of Trips	No. of People	Duration	Airfare	Per Diem	Total
15	Vancouver, BC, Canada	TIMs	1	2	3	$375	$343	$2,808
							FY 15 Subtotal	**$2,808**
16	Grand Canyon, AZ	Workshop on Superconducting Electronics	1	1	5	$507	$239	$1,702
16	Minneapolis, MN	TIMs	1	2	3	$507	$239	$2,448
16	Charlotte, NC	Applied Superconductivity Conference	1	2	6	$507	$239	$3,882
							FY 16 Subtotal	**$8,032**
17	Vancouver, BC, Canada	TIMs	1	2	3	$399	$365	$2,988
							FY 17 Subtotal	**$2,988**
							Total	**$13,828**


Web
Flights
Hotels
More
Round trip
One way
Multi-city
Economy
LAX Los Angeles
to
YVR Vancouver
Mon, June 9
to
Thu, June 12
Stops
Price
Airlines
Times
More
Los Angeles – Vancouver Mon, Jun 9
Sort by Price round trip
12:45 pm —3h— Alaska / Delta, American Nonstop from $364
2:15 pm —3h— WestJet / American Nonstop from $364
12:15 pm —3h— Air Canada / United Nonstop from $364
3:05 pm —3h— Alaska / Delta, American Nonstop from $364
4:16 pm —3h— United / Air Canada Nonstop from $364
Alaska / Delta, American Nonstop from $364
6:41 pm —3h— Air Canada / United Nonstop from $364
10:18 pm —3h— Air Canada / United Nonstop from $364
10:33 pm —3h— WestJet / American Nonstop from $364
11:39 pm —3h— Alaska / Delta, American Nonstop from $364

FY15 Vancouver, Canada, per diem rate: $333*1.023 = $341

Country Name	Post Name	Season Begin	Season End	Maximum Lodging Rate	M & IE Rate	Maximum Per Diem Rate	Footnote	Effective Date
CANADA	St. John's, Newfoundland	01/01	12/31	170	113	283	N/A	08/01/2013
CANADA	Toronto	01/01	12/31	200	115	315	View	08/01/2013
CANADA	Vancouver	05/01	10/15	212	121	333	N/A	08/01/2013
CANADA	Vancouver	10/16	04/30	183	118	301		
CANADA	Victoria	05/01	10/15	226	134	362	N/A	08/01/2013

Maximum Per Diem Rate

3. Services

FY	Vendor	Description	Source	Total Amount
15	JPL	MDL Beneficiary Fee	JPL Published Rates	$2,000
15	JPL	MDL Family Member	JPL Published Rates	$2,500
15	JPL	MDL Annual Task Fee	JPL Published Rates	$17,500
			FY 15 Subtotal	**$22,000**
16	JPL	MDL Beneficiary Fee	JPL Published Rates	$2,000
16	JPL	MDL Family Member	JPL Published Rates	$2,500
16	JPL	MDL Annual Task Fee	JPL Published Rates	$17,500
			FY 16 Subtotal	**$22,000**
17	JPL	MDL Beneficiary Fee	JPL Published Rates	$2,000
17	JPL	MDL Family Member	JPL Published Rates	$2,500
17	JPL	MDL Annual Task Fee	JPL Published Rates	$17,500
			FY 17 Subtotal	**$22,000**
			Total	**$66,000**

4. Procurements

FY	Vendor	Description	Source	Number Units/Hrs	Cost per Unit/Hrs	Escalation	Total Amount
15	TBD - Various vendors depending on availability	Consumables wafers, chemicals, tools, components, minor lab substrates, targets, vacuum parts, masks, test equipment.	Engineering Estimate	1	$36,000	1.00	$36,000
						FY 15 Subtotal	**$36,000**
16	TBD - Various vendors depending on availability	Consumables wafers, chemicals, tools, components, minor lab substrates, targets, vacuum parts, masks, test equipment.	Engineering Estimate	1	$36,000	1.00	$36,000
						FY 16 Subtotal	**$36,000**
17	TBD - Various vendors depending on availability	Consumables wafers, chemicals, tools, components, minor lab substrates, targets, vacuum parts, masks, test equipment.	Engineering Estimate	1	$36,000	1.00	$36,000
						FY 17 Subtotal	**$36,000**
						Total	**$108,000**

5. Subcontracts

There will be no subcontracts for this effort.

6. Chargebacks

Chargebacks account for Enterprise Information System (EIS) costs which consist of telephone, paging, file and message services and Desktop and Network Services (DNS). Desktop and Network Services (DNS) costs consist of network and desktop computer-related charges. Chargebacks are calculated as a rate per direct labor hour. The rate is published as part of JPL's rate package (Rate version FY14-2).

Fiscal Year	FY 15	FY 16	FY 17	Total
Total Labor Hours	1,437	1,437	1,437	4,311
Rate	$6.16	$6.16	$6.16	$6.16

TOTAL	**$8,851**	**$8,851**	**$8,851**	**$26,553**

COST ESTIMATE (expressed in whole dollars)

	Previously Proposed	Revision A FY15	Revision A FY16	Revision A FY17	Revision A Total	Task Plan Total
1. Workhours						
JPL Hours	13537	1437	1437	1437	4311	17848
Cat A Hours	0	0	0	0	0	0
2. Total Direct Compensation (includes Employee Benefits)	$1,228,914	$146,338	$151,694	$158,064	$456,096	$1,685,010
3. Travel	$21,676	$2,808	$8,032	$2,988	$13,828	$35,504
4. JPL Services	$263,250	$22,000	$22,000	$22,000	$66,000	$329,250
5. Procurements						
Chargebacks	$73,101	$8,851	$8,851	$8,851	$26,553	$99,654
Subcontracts	$0	$0	$0	$0	$0	$0
Procurement RSA	$0	$0	$0	$0	$0	$0
Purchases Orders	$117,000	$36,000	$36,000	$36,000	$108,000	$225,000
Procurement IA	$0	$0	$0	$0	$0	$0
Caltech Transfers	$0	$0	$0	$0	$0	$0
6. Multi-Program Support	$169,594	$16,741	$15,936	$16,055	$48,732	$218,327
7. Total Direct Costs	$1,873,535	$232,738	$242,513	$243,958	$719,209	$2,592,744
8. Allocated Direct Charge	$599,039	$80,697	$80,128	$81,087	$241,912	$840,951
9. Total JPL Costs	$2,472,574	$313,435	$322,641	$325,045	$961,122	$3,433,695
10. NASA Costs	$83,519	$19,996	$20,583	$20,737	$61,316	$144,835
11. **Total Estimated Cost**	$2,556,093	$333,431	$343,224	$345,782	$1,022,437	$3,578,530

Additional Documentation:

D-Wave Task Plan 82-16404, Rev. A
JPL Project/Task 104853-1.1
Budget Notes

Task Plan dates

- Original Task Plan 6/22/2011 – 9/28/2014
- Revised Task Plan 6/22/2011 – 9/24/2017 (extend by 3 years)

We need a budget for the period 9/29/2013 – 9/24/2017 (FY 2014 – FY 2017)

Total Funding

- Total funding (original Task Plan) $2,556,093
- Total funding (revised Task Plan) $3,578,530 (increase of $1,022,437 or 40%)

Current funding

- Total received from D-Wave to date $1,600,000
- Total expended through FY 2013 $1,285,405 (estimated, including $75,729 in NASA taxes)
- Total remaining 9/28/20 $314,595 (estimated)

  The remaining total is estimated based on spending through 9/15/13
  The total needs to be updated after FY 2013 closes

Future Funding

- Additional future funding $2,293,125 ($573,281/year)

  $3,578,530 (new Task total) - $1,600,000 (already received) + $314,595 (estimated remaining)

So, we need a budget for FY 2014 – FY 2017 that totals $2,309,110 (subject to small correction after close of FY 2013)

Budget input on following page

PEG budget attached

- Budget target: $2,309,110
- PEG actual: $2,314.910
    - FY14: $527.74K
    - FY15: $569.91K
    - FY16: $616.81K
    - FY17: $600.45K

Budget input

- Personnel
  - Alan Kleinsasser 389I Engineering 4 0.8 FTE
  - Talso Chui 385J Engineering 4 0.5 FTE
  - Bruce Bumble 389I Engineering 4 0.2 FTE
- MDL Fees: Add the following 3 items (Total $81K)
  - $25K (annual task fee for tasks with 1 FTE or more)
  - MDL Family charges: FTE * $25K = 0.2*$25K = $5K
  - MDL Beneficiary charges: FTE * $5K = $0.8*$5K = $4K
    389I Group Supervisor hours automatically allocated – approximately 10% of MDL Family hours
- Travel
  - Workshop on Superconducting Electronics, Grand Canyon, AZ, October 20-24, 2013 (Conference)
    - 1 person, 5 days/5 nights ($1600 total)
  - Cypress Semiconductor, Minneapolis, MN, June 2014 (Programmatic)
    - 2 people, 3 days/2 nights ($1500 per person)
  - Applied Superconductivity Conference, Charlotte, NC, August 2014 (Conference)
    - 2 people, 6 days/6 nights ($2000 per person)
  - D-Wave Systems Inc., Vancouver, BC, Canada, June 2015 (Programmatic)
    - 2 people, 3 days/2 nights ($1500 per person)
  - Workshop on Superconducting Electronics, October 2015 (Conference)
    - 1 person, 5 days/5 nights ($1600 total)
  - Cypress Semiconductor, Minneapolis, MN, June 2016 (Programmatic)
    - 2 people, 3 days/2 nights ($1500 per person)
  - Applied Superconductivity Conference, August 2016 (Conference)
    - 2 people, 6 days/6 nights ($2000 per person)
  - D-Wave Systems Inc., Vancouver, BC, Canada, June 2017 (Programmatic)
    - 2 people, 3 days/2 nights ($1500 per person)
- Procurements
  - Various vendors depending on availability
  - Consumables wafers, chemicals, tools, components, minor lab substrates, targets, vacuum parts, masks, test equipment
  - Engineering Estimate based on current level of effort for this task
  - $3K/month

SPACE ACT AGREEMENT

BETWEEN THE

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

AND

D-WAVE SYSTEMS INC.

FOR

ADIABATIC QUANTUM COMPUTING

FABRICATION PROCESS DEVELOPMENT

ARTICLE 1. AUTHORITY

This Agreement is entered into by the National Aeronautics and Space Administration, represented by the NASA Management Office, located at the Jet Propulsion Laboratory, Pasadena, CA 91109 (hereinafter referred to as "NASA"), pursuant to the National Aeronautics and Space Act of 1958, including 51 U.S.C. Section 20113, and D-Wave Systems Inc. with a place of business at 100-4401 Still Creek Drive, Burnaby, British Columbia V5C 6G9 Canada. The term "Party" or "Parties" may be used herein to refer to one or both of the above referenced entities.

ARTICLE 2. DEFINITIONS

1. "Related Entity", as used herein, means a contractor, subcontractor, grantee, or other entity having a legal relationship with NASA or D-Wave Systems Inc. that is assigned, tasked, or contracted with to perform specified NASA or D-Wave Systems Inc. activities under this Agreement.

2. "Data", as used herein, means recorded information, regardless of form, the media on which it may be recorded, or the method of recording. The term includes, but is not limited to, data of a scientific or technical nature, computer software and documentation thereof, and data comprising commercial and financial information.

3. "Proprietary Data", as used herein, means Data embodying trade secrets or comprising commercial or financial information that is privileged or confidential and is marked with a suitable restrictive notice.

4. "Scientific and Technical Articles", as used herein, means scientific and technical articles based on or containing Data first produced by the California Institute of Technology (Caltech) in the performance of NASA contract NAS7-03001 and published in academic, technical, or professional journals, symposia proceedings or similar works.

5. "Protected Computer Software", as used herein, means copyrighted or patented Data embodied in source or object code or software documentation first produced by Caltech under contract NAS7-03001 for NASA and pursuant to this Agreement. Protected Computer Software is the property of Caltech and any use of such Protected Computer Software other than as authorized herein must be negotiated with the Office of Technology Transfer at Caltech.

ARTICLE 3. PURPOSE AND AGENCY COMMITMENT

See Task Plan No. 82-16404, incorporated herein.

ARTICLE 4. RESPONSIBILITIES

See Task Plan No. 82-16404, incorporated herein.

ARTICLE 5. SCHEDULE AND MILESTONES

See Task Plan No. 82-16404, incorporated herein.

ARTICLE 6. FINANCIAL OBLIGATIONS

See Task Plan No. 82-16404, incorporated herein.

1. There shall be a transfer of funds from D-Wave Systems Inc. to NASA in connection with this Agreement. The Parties agree that the terms of reimbursement for NASA's participation shall be as specified below.

2. D-Wave Systems Inc. agrees to reimburse NASA an estimated cost of **$2,566,093** to carry out its responsibilities under this Agreement. Payment must be made by D-Wave Systems Inc. in advance of initiation of NASA's efforts.

3. An invoice will be submitted to D-Wave Systems Inc. for the initial incremental payment and thereafter no later than 45-days prior to exhaustion of funds. The proposed payment schedule will be the following:

Initial payment authorized to proceed	Due at contract start date	$200,000
Incremental funds	Due 3 months after contract start date	$200,000
Incremental funds	Due 6 months after contract start date	$200,000
Incremental funds	Due 9 months after contract start date	$200,000
Incremental funds	Due 12 months after contract start date	$200,000
Incremental funds	Due 15 months after contract start date	$200,000
Incremental funds	Due 18 months after contract start date	$200,000
Incremental funds	Due 21 months after contract start date	$200,000
Incremental funds	Due 24 months after contract start date	$200,000
Incremental funds	Due 27 months after contract start date	$200,000
Incremental funds	Due 30 months after contract start date	$200,000
Incremental funds	Due 33 months after contract start date	$200,000
Incremental funds	Due 36 months after contract start date	$156,093
TOTAL		**$2,556,093**

Advance payments shall be scheduled to ensure that funds are resident with NASA before Federal obligations are incurred in support of this Agreement

4. Payment shall be payable to the National Aeronautics and Space Administration through the NASA Shared Services Center (NSSC) via: [*1*] U.S. Treasury FEDWIRE Deposit System, Federal Reserve Wire Network Deposit System, pay.gov at: https://www.nssc.nasa.gov/portal/site/customerservice/menuitem.bb29c518138071c056969daf4dd72749; *or* [*2*] check. A check should be payable to NASA and sent to: NASA Shared Services Center; FMD – Accounts Receivable; For the Accounts of: NASA/Jet Propulsion Laboratory (attention: Mr. Brian Landry); Bldg 1111, C Road; Stennis Space Center, MS 39529. Payment by electronic transfer is strongly encouraged, and payment by check is to be used only if circumstances preclude the use of electronic transfer. All payments and other communications regarding this Agreement shall reference the Center name, title, date, and number of this Agreement.

5. Whichever method D-Wave Systems Inc. uses to submit the payment, D-Wave Systems Inc. will alert the JPL Contract Administrator, Mr. Robert R. Chan, of the payment by sending an email to him at: rrchan@jpl.nasa.gov.

6. NASA will not provide services or incur costs beyond the available funding amount. Although NASA has made a good faith effort to accurately estimate its costs, it is understood that NASA provides no assurance that the proposed effort under this Agreement will be accomplished for the above estimated amount. Should the effort cost more than the estimate, D-Wave Systems Inc. will be advised by NASA as soon as possible. D-Wave Systems Inc. shall pay all costs incurred and has the option of canceling the remaining effort, or providing additional funding in order to continue the proposed effort under the revised estimate. Should this Agreement be terminated, or the effort completed at a cost less than the agreed-to estimated cost, NASA shall account for any unspent funds after completion of all effort under this Agreement, and promptly thereafter return any unspent funds to D-Wave Systems Inc.

ARTICLE 7. SCHEDULING CONFLICTS

The schedule and milestones identified herein are estimated based upon the parties' current understanding of the projected use of NASA resources. In the event NASA's projected usage changes, D-Wave Systems Inc. shall be given reasonable notice of the change, so that the schedule and milestones may be adjusted accordingly. The parties agree that NASA's or the U.S. Federal Government's usage of the test facilities and equipment shall have priority over the usage planned in this Agreement, should a conflict arise, and NASA, at its sole discretion, shall determine whether to exercise that priority. Likewise, should a conflict arise between two or more users, NASA, at its sole discretion, shall determine the priority between the two users.

ARTICLE 8. NONEXCLUSIVITY

This agreement is not exclusive; accordingly, NASA may enter into similar agreements for the same or similar purpose with other private or public entities.

ARTICLE 9. PROPERTY

Non-Deliverable Tangible Property. All tangible property produced or acquired under this Agreement that is not a deliverable pursuant to the Responsibilities and Schedules/Milestones herein shall become the property of NASA. At the conclusion of work under this Agreement, for tangible property that is solely funded by D-Wave Systems Inc., NASA will transfer ownership to D-Wave Systems Inc. at D-Wave Systems Inc.'s written request. Upon such request, D-Wave Systems Inc. shall take possession of its tangible property and bear the costs of the removal and transportation to its own facility. Any transportation or disposal of property shall be in accordance with applicable Federal, State, and local requirements.

Deliverable Tangible Property. Ownership for all tangible property produced or acquired under this Agreement that is a deliverable pursuant to the attached Task Plan herein shall remain with NASA until completion of the attached Task Plan or termination of this Agreement. Upon completion of the attached Task Plan or termination of this Agreement, NASA will effect transfer of ownership of all such tangible property to D-Wave Systems Inc.

ARTICLE 10. EXPORT CONTROL

Compliance. The parties acknowledge and agree that this Agreement is subject in all respects to the laws and regulations of the United States, including the Export Administration Act of 1979 (50 U.S.C. app. 2401, et seq.), as amended, and the Arms Export Control Act (22 U.S.C. 2778), as amended, and all regulations thereunder, including the International Traffic in Arms Regulations (22 C.F.R. 120-130), as amended, and Export Administration Regulations (15 C.F.R. 730-774), as amended. The parties understand that information and technology resulting from the performance of this Agreement may be subject to export control laws and regulations, and each party is responsible for its own compliance with such laws and regulations. Nothing in

this Agreement waives any such statutory or regulatory requirement. The parties further acknowledge that export control restrictions may impact NASA's ability to perform the work and/or may result in delays in any planned deliverables and D-Wave Systems Inc. agrees that NASA shall not be responsible to D-Wave Systems Inc. for any resulting inability to perform and/or delays.

Disclosure of Export Controlled Goods and Technical Data. If a party or its contractor(s) discloses specifically identified or marked goods or technical data subject to U.S. export laws and regulations to the other party under this Agreement, the receiving party agrees that such technical data will not be further provided to foreign persons, as defined in 22 C.F.R. 120.16, or be shipped or transmitted outside the United States without proper U.S. Government authorization, where required. The receiving party agrees that export-controlled goods and technical data will be used only for the purpose of fulfilling the receiving party's responsibilities under this Agreement.

ARTICLE 11. LIABILITY AND RISK OF LOSS

1. Each Party hereby waives any claim against the other Party, employees of the other Party, the other Party's Related Entities or employees of the other Party's Related Entities for any injury to, or death of, the waiving Party's employees or the employees of its Related Entities, or for damage to, or loss of, the waiving Party's property or the property of its Related Entities arising from or related to activities conducted under this Agreement, whether such injury, death, damage, or loss arises through negligence or otherwise, except in the case of willful misconduct.

2. Each Party further agrees to extend this cross-waiver to its Related Entities by requiring them, by contract or otherwise, to waive all claims against the other Party, Related Entities of the other Party, and employees of the other Party or of its Related Entities for injury, death, damage, or loss arising from or related to activities conducted under this Agreement. Additionally, each Party shall require that their Related Entities extend this cross-waiver to their Related Entities by requiring them, by contract or otherwise, to waive all claims against the other Party, Related Entities of the other Party, and employees of the other Party or of its Related Entities for injury, death, damage, or loss arising from or related to activities conducted under this Agreement.

ARTICLE 12. INTELLECTUAL PROPERTY & DATA RIGHTS – RIGHTS IN DATA

1. General:

(a) The Data rights set forth herein are applicable to employees of NASA and D-Wave Systems Inc. and employees of any Related Entity of NASA and D-Wave Systems Inc. NASA and D-Wave Systems Inc. shall ensure that its employees and employees of any Related Entity that perform activities under this Agreement are aware of the obligations under this Article 12 and that all such employees are bound to such obligations.

(b) Data exchanged between NASA and D-Wave Systems Inc. under this Agreement will be exchanged without restriction as to its disclosure, use, or duplication except as otherwise provided in this Agreement.

(c) No preexisting Proprietary Data or Data protected by copyright or patent will be exchanged between the parties under this Agreement unless specifically authorized in this Article 12 or in writing by the owner of the Proprietary Data or Data protected by copyright or patent.

(d) In the event that Data exchanged between NASA and D-Wave Systems Inc. includes a restrictive notice that NASA or D-Wave Systems Inc. deems to be ambiguous or unauthorized, NASA or D-Wave Systems Inc. may inform the other party of such condition. Notwithstanding such a notice, as long as such notice provides an indication that a restriction on use or disclosure was intended; the party receiving such Data will treat the Data pursuant to the requirement of this Article 12 unless otherwise directed in writing by the party providing such Data.

(e) Notwithstanding any restriction on use, disclosure, or reproduction of Data provided in this Article 12, the parties or their Related Entities will not be restricted in the use, disclosure, or reproduction of Data provided under this Agreement that: (i) is publicly available at the time of disclosure, or reproduction of Data provided under this Agreement that: (i) is publicly available at the time disclosure or thereafter becomes publicly available without breach of this Agreement; (ii) is known to, in the possession of, or developed by the receiving party independent of any disclosure of, or without reference to, Proprietary Data or otherwise protectable Data hereunder; (iii) is received from a third party having the right to disclose such information with restriction; or (iv) is required to be produced or released by the receiving party pursuant to a court order or other legal requirement.

(f) If either NASA or D-Wave Systems Inc. believes that any of the events or conditions that remove restriction on the use, disclosure, or reproduction of the Data apply, NASA or D-Wave Systems Inc. will promptly notify the other party and any affected Related Entity of such belief prior to acting on such belief, and, in any event, will notify the other party and any affected Related Entity prior to an unrestricted use, disclosure, or reproduction of such Data.

(g) Disclaimer of Liability: Notwithstanding any restriction on use, disclosure, or reproduction of Data provided in this Article 12, NASA or any NASA Related Entity will not be restricted in, nor incur any liability for, the use, disclosure, or reproduction of any Data not identified with a suitable restrictive notice in accordance with this Agreement or of any Data included in Data which D-Wave Systems Inc. or any D-Wave Systems Inc. Related Entity has furnished, or is required to furnish to the U.S. Government without restriction on disclosure and use.

(h) D-Wave Systems Inc. or any Related Entity may use the following, or a similar, restrictive notice as required by paragraphs 2 and 8 of this Article. In addition to identifying Proprietary Data with such a restrictive notice, D-Wave Systems Inc. should mark each page containing Proprietary Data with the following, or a similar legend: "Proprietary Data – use and disclose only in accordance with notice on title or cover page."

Sample Proprietary Data Notice:

> "These data herein include *<enter as applicable*: "Background Data" or "Data Produced by D-Wave Systems Inc./ [Related Entity] under a Space Act

Agreement"> in accordance with the Data Rights provisions under the Space Act Agreement 82-16404 and embody Proprietary Data"

2. Data First Produced by D-Wave Systems Inc. under this Agreement:

In the event Data first produced by D-Wave Systems Inc. in carrying out the responsibilities of D-Wave Systems Inc. under this Agreement is furnished to NASA or a NASA Related Entity, and D-Wave Systems Inc. considers such Data to be Proprietary Data, and such Data is identified with a suitable restrictive notice, NASA will use reasonable efforts to maintain the Data in confidence and such Data will be disclosed and used by NASA and any Related Entity of NASA (under suitable protective conditions) only for government or internal research purposes. D-Wave Systems Inc. herein grants NASA and NASA Related Entities an irrevocable, royalty-free license to all Data first produced by D-Wave Systems Inc. or D-Wave Systems Inc.'s Related Entities under this Agreement for non-commercial, government purposes.

3. Data First Produced by NASA under this Agreement:

(a) In the event D-Wave Systems Inc. requests that Data first produced by NASA (or any Related Entity of NASA) in carrying out NASA responsibilities under this Agreement be maintained in confidence, and NASA determines that such Data would be Proprietary Data if it had been obtained from D-Wave Systems Inc., NASA or a NASA Related Entity will mark such Data with a restrictive notice and will maintain such marked Data in confidence for the duration of this Agreement, with the express understanding that during the aforesaid restricted period such marked Data may be disclosed and used by NASA and any Related Entity of NASA (under suitable protective conditions) only for government or internal research purposes.

(b) Protected Computer Software and Scientific and Technical Articles developed pursuant to this Agreement are the property of Caltech and any use of such Protected Computer Software or Scientific and Technical Articles other than as authorized by this Article 12, Paragraph 6, Copyright or Article 13. Intellectual Property and Data Rights, Patents and Inventions, must be negotiated with the Office of Technology Transfer at Caltech.

4. Publication of Results:

It is recognized by the parties that section 203 of the National Aeronautics and Space Act of 1958 (42 U.S.C. § 2473), as amended, requires NASA to provide for the widest practicable and appropriate dissemination of information concerning its activities and the results thereof, and that the dissemination of the results of NASA activities is one of the considerations for this Agreement. As such, subject to applicable U.S. Export Control laws, NASA or NASA Related Entities shall have the right to publish the unclassified and non-Proprietary Data resulting from work performed under this Agreement. In accordance with Article 13, reasonable precautions will be taken to safeguard against disclosure of potentially patentable inventions. NASA shall provide D-Wave Systems Inc. a copy of proposed publications no later than simultaneously with release for publication.

5. Data Disclosing an Invention:

In the event Data is exchanged between NASA (or NASA Related Entities) and D-Wave Systems Inc. that discloses an invention for which patent protection is being considered, the furnishing party specifically identifies such Data, and the disclosure and use of such Data is not otherwise limited or restricted herein, the receiving party agrees to withhold such Data from public disclosure for a reasonable time in order for a patent application filing to be made.

6. Copyright:

In the event Data is exchanged with a notice indicating that the Data is copyrighted and there is no indication that such Data is subject to restriction under paragraphs 1-3 of this Article 12 (i.e., Data is not marked with a restrictive notice as required by paragraphs 1-3 of this Article 12), such Data will be presumed to be published and the following royalty-free licenses will apply:

(a) If it is indicated on the Data that the Data existed prior to, or was produced outside of, this Agreement, the receiving party and others acting on its behalf, may reproduce, distribute, and prepare derivative works only for carrying out the receiving party's responsibilities under this Agreement.

(b) If the Data does not contain the indication of (a) above, the Data will be presumed to have been first produced under this Agreement and, except as otherwise provided in paragraph 3(b) or 5 of this Article 12 and in the Inventions and Patent Rights Article 13 of this Agreement for protection of copyrighted material or reported inventions, the receiving party and others acting on its behalf may reproduce, distribute, and prepare derivative works for any purpose.

(c) If the Data is produced by Caltech under contract NAS7-03001 for NASA pursuant to this Agreement and is funded in part or in whole by D-Wave Systems Inc., D-Wave Systems Inc. shall receive a royalty-free, non-exclusive, non-commercial, internal use license on behalf of the U.S. Government pursuant to contract NAS7-03001. Sublicenses shall not be permitted by D-Wave Systems Inc.. Inquiries regarding commercial or exclusive licenses should be directed to Caltech's Office of Technology Transfer through the Commercial Programs Office at JPL (818) 354-3821.

7. Data Subject to Export Control:

Consistent with Article 10 herein, specifically identified or marked technical data that is subject to the export laws and regulations of the United States and that is provided to D-Wave Systems Inc. under this Agreement will be treated as such, and will not be further provided to any foreign persons or transmitted outside the United States without proper U.S. Government authorization, where required.

8. Background Data:

(a) In the event the parties or their Related Entities furnish to the other party Data developed at private expense that existed prior to, or was produced outside of, this Agreement, and such Data embody Proprietary Data or Data protected by copyright, and such Data is so identified with a suitable restrictive notice, the parties and their Related Entities will use reasonable efforts to maintain the Data in confidence and such Data will be disclosed and used

by the parties and their Related Entities (under suitable protective conditions) only for carrying out responsibilities under this Agreement, upon completion of activities under this Agreement, such Data will be disposed of as requested by the provider of the Data. If such Data cannot be separated from Data produced under this Agreement, the Parties and any Related Entities with an ownership interest in such Data agree to negotiate an appropriate license for the use of such Data.

(b) The Parties and their Related Entities agree that the following Background Data which embodies Proprietary Data or Data protected by copyright may be used in the performance of this Agreement. This list may not be comprehensive, is subject to change during the course of the Agreement, and is not meant to supersede any restrictive markings which may be on Data provided: **TBD.**

9. Handling of Data:

(a) In the performance of this Agreement, D-Wave Systems Inc. and any Related Entity of D-Wave Systems Inc. may have access to, be furnished with, or use the following categories of Data:

(i) Proprietary Data of NASA Related Entities, third parties that the U.S. Government has agreed to handle under protective arrangements;
(ii) U.S. Government Data, the use and dissemination of which, the U.S. Government intends to control; and/or,
(iii) Data protected by copyright, including Protected Computer Software.

(b) Data provided by the U.S. Government under the Agreement:

(i) The parties agree that the following Proprietary Data of NASA Related Entities or third parties may be provided to D-Wave Systems Inc. with the express understanding that D-Wave Systems Inc. will use and protect such Proprietary Data in accordance with Articles 12 and 13. This list may not be comprehensive, is subject to change during the course of the work under this Agreement, and is not meant to supersede any restrictive markings which may be on Data provided: **TBD**
(ii) The parties agree that the following U.S. Government Data may be provided to D-Wave Systems Inc. with the express understanding that D-Wave Systems Inc. will use and protect such U.S. Government Data in accordance with this clause: **TBD**
(iii) Except as otherwise provided in this Agreement, the parties agree that the following Protected Computer Software may be provided to D-Wave Systems Inc. under a separate license with the express understanding that D-Wave Systems Inc. will use and protect such Protected Computer Software in accordance with Articles 12 and 13. This list may not comprehensive is subject to change during the course of the work under this Agreement, and is not meant to supersede any restrictive markings which may be on Data provided: **TBD**

(c) With respect to any Data specifically marked with a restrictive notice, D-Wave Systems Inc. agrees to:

(i) Use, disclose, or reproduce such Data only to the extent necessary to perform the work required under this Agreement;

(ii) Safeguard such Data from unauthorized use and disclosure;
(iii) Allow access to such Data only to its employees and any Related Entity that require access for their performance under this Agreement.
(iv) Except as otherwise indicated in (c) (iii) above, preclude access and disclosure of such Data outside D-Wave Systems Inc.'s organization;
(v) Notify its employees who may require access to such Data about the obligations under Articles 12 and 13, administer a monitoring process to ensure that such employees comply with such obligations, and ensure that any Related Entity perform as the same functions with respect to its employees; and,
(vi) Return or dispose of such Data, as NASA or a NASA Related Entity may direct, when the Data is no longer needed for performance under this Agreement.

(d) In the event that access to, acquisition of, or delivery of classified material is required under this Agreement, D-Wave Systems Inc. must provide a completed Contract Security Classification Specification (DD Form 254 or equivalent) to the NASA Management Office at the following address:

Attn: Raymond Wilkens, Contracting Officer
National Aeronautics and Space Administration
NASA Management Office – JPL
4800 Oak Grove Drive, Mail Stop 180-802
Pasadena, CA 91109

Transmission and access to classified material shall be in accordance with NASA and U.S. Federal Government statutes, regulations, and policies.

10. Oral and Visual Information:

If information that D-Wave Systems Inc. considers to be Proprietary Data is disclosed orally or visually to NASA or a NASA Related Entity, NASA will have no duty to limit or restrict, and will not incur any liability for, any disclosure or use of such information unless (a) D-Wave Systems Inc. orally informs NASA or a Related Entity before initial disclosure that such information is considered to be Proprietary Data, and (b) D-Wave Systems Inc. reduces such information to tangible, recorded form that is identified and marked with a suitable restrictive notice as required by paragraphs 1, 2 and 8 above and furnishes the resulting Data to NASA or a NASA Related Entity within 10 days after such oral or visual disclosure.

ARTICLE 13. INTELLECTUAL PROPERTY AND DATA RIGHTS – RIGHTS IN INVENTIONS AND PATENTS

1. General:

(a) Based on the purpose and scope of this Agreement, and the responsibilities of the parties, NASA has made an administrative determination that the National Aeronautics and Space Act of 1958 51 U.S.C. § 20135(b), do not apply to this Agreement. Therefore, title to inventions made (conceived or first actually reduced to practice) as a result of activities

performed under this Agreement will remain with the respective inventing party(ies), and no invention or patent rights are exchanged between or granted by such parties under this Agreement except as provided herein.

(b) The invention and patent rights set forth herein are applicable to employees of D-Wave Systems Inc. and employees of any Related Entity of D-Wave Systems Inc.. D-Wave Systems Inc. shall ensure that its employees and employees of any Related Entity that perform activities of D-Wave Systems Inc. under this Agreement are aware of the obligations under this Article 13 and that all such employees are bound to such obligations.

2. NASA Inventions:

Upon request, NASA will use reasonable efforts to grant D-Wave Systems Inc., consistent with the requirements of 37 C.F.R. Part 404, a license, on terms to be subsequently negotiated to any NASA invention made as a result of activities performed under this Agreement on which NASA decides to file a patent application. This license will be subject to the rights reserved in paragraph 5(a) below.

3. NASA Related Entity Inventions:

(a) In the event that inventions are made under this Agreement by employees of a NASA Related Entity or jointly between NASA employees and employees of a NASA Related Entity, and NASA has the right to acquire or has acquired title to such inventions, NASA will use reasonable efforts to report such inventions. Upon request, NASA will use reasonable efforts to grant D-Wave Systems Inc., consistent with the requirements of 37 C.F.R. Part 404, a license on terms to be subsequently negotiated to any such invention on which NASA has acquired title and decides to file a patent application. This license will be subject to the rights reserved in paragraph 5(b) below.

(b) For inventions made as a result of activities performed under this Agreement, elected upon by Caltech pursuant to contract NAS7-03001 with NASA at the Jet Propulsion Laboratory, and funded in part or in whole by D-Wave Systems Inc., D-Wave Systems Inc. shall receive a royalty-free, non-exclusive, non-commercial, internal use license to such inventions. Sub-licenses shall not be permitted by D-Wave Systems Inc.. Caltech shall consider and, if appropriate under the current Caltech policy, may grant D-Wave Systems Inc. greater license rights or an option to greater license rights than those provided herein under mutually agreeable terms and conditions. Such terms and conditions shall be negotiated by D-Wave Systems Inc. and Caltech Office of Technology Transfer through the Commercial Programs Office at JPL (818) 354-3821 pursuant to a separate agreement.

4. Joint Inventions With D-Wave Systems Inc.:

NASA and D-Wave Systems Inc. agree to use reasonable efforts to identify and report to each other, and to cooperate with each other in obtaining patent protection on, any inventions made jointly between NASA employees (or employees of a NASA Related Entity) and employees of D-Wave Systems Inc.. To the extent that NASA has the right to or has acquired title in such

joint inventions, and upon timely request by D-Wave Systems Inc., NASA may, at its sole discretion and subject to the applicable rights reserved in paragraph 5 below:

(a) Agree to refrain from exercising its undivided interest in a manner inconsistent with D-Wave Systems Inc.'s commercial interests; or

(b) use reasonable efforts to grant D-Wave Systems Inc., consistent with the requirements of 37 C.F.R. Part 404, an exclusive or partially exclusive license on terms to be subsequently negotiated to NASA's undivided interest in such joint inventions.

(c) For inventions made jointly between D-Wave Systems Inc. and Caltech, pursuant to contract NAS7-03001, provisions of Article 12, paragraph 3(b) apply.

5. Rights to be Reserved in D-Wave Systems Inc.'s License:

Any license granted to D-Wave Systems Inc. pursuant to paragraphs 2, 3, or 4 above will be subject to the reservation of the following rights:

(a) As to inventions made solely or jointly by NASA employees, NASA reserves the irrevocable, royalty-free right of the Government of the United States to practice the invention or have the invention practiced on behalf of the United States or on behalf of any foreign government or international organization pursuant to any existing or future treaty or agreement with the United States. NASA will use reasonable efforts to limit use of the invention to use by or on behalf of NASA for research, experimental, or evaluation purposes.

(b) As to inventions made solely or jointly by employees of a NASA Related Entity, other than Caltech, NASA reserves the rights as set forth in (a) above, as well as the revocable, nonexclusive, royalty-free license in the Related Entity as set forth in 14 C.F.R. §1245.108 or 37 C.F.R. § 401.14(e), as applicable.

(c) As to inventions made solely or jointly by employees of Caltech and elected upon by Caltech pursuant to contract NAS7-03001 with NASA at the Jet Propulsion Laboratory, Caltech retains exclusive ownership, subject to the rights reserved by NASA under contract NAS7-03001 and provided to D-Wave Systems Inc. herein.

6. Protection of Reported Inventions:

When inventions are reported and disclosed between the parties in accordance with the provisions of this Article 13, the receiving party agrees to withhold such reports or disclosures from public access for a reasonable time in order to facilitate the allocation and establishment of the invention and patent rights under these provisions.

7. Patent Filing Responsibilities and Costs:

(a) The invention and patent rights set forth herein will apply to any patent application filed and any patent obtained covering an invention made as a result of the performance of activities under this Agreement. Each party is responsible for its own costs of obtaining and maintaining patents covering sole inventions of its employees; except that NASA, to the extent it has the right to acquire or has acquired title of the invention and patent rights, and D-Wave

Systems Inc. may mutually agree otherwise, upon the reporting of any invention (sole or joint) or in any license granted, as to responsibilities and costs of obtaining and maintaining patents.

(b) D-Wave Systems Inc. agrees to include the following statement in any patent application it files for an invention made jointly between NASA employees (or employees of a NASA Related Entity) and employees of D-Wave Systems Inc.: "The invention described herein may be manufactured and used by or for the U.S. Government for U.S. Government purposes without the payment of royalties thereon or therefore."

(c) For joint inventions developed between D-Wave Systems Inc. and Caltech, which Caltech has elected to file a patent application pursuant to NAS7-03001, D-Wave Systems Inc. and Caltech shall negotiate terms of ownership, filing responsibilities, and costs in a separate agreement.

8. Related Inventions:

(a) For the purposes of this paragraph, a Related Invention is an invention related to the subject matter of this Agreement, but not made as a result of activities performed under this Agreement, that is covered by a patent application or patent owned by NASA, a NASA Related Entity, or D-Wave Systems Inc..

(b) No preexisting Related Inventions will be exchanged between the parties under this Agreement unless specifically authorized in this Article 13 or in writing by the owner of the Related Inventions.

(c) To the extent NASA Related Invention(s) are known, and to the extent such related inventions are available for licensing, NASA may enter into negotiations with D-Wave Systems Inc. for a license to such related invention(s) consistent with the requirements of 37 C.F.R. Part 404.

(d) For Related Inventions owned by D-Wave Systems Inc., D-Wave Systems Inc. grants to NASA and NASA Related Entities a non-exclusive, royalty-free license to use the Related Inventions in order to perform under this Agreement. If D-Wave Systems Inc.'s Related Inventions can be separated from inventions produced under this Agreement, upon completion of activities under this Agreement, such D-Wave Systems Inc. Related Inventions will be returned to D-Wave Systems Inc. and the license to use the Related Inventions herein will expire. If such D-Wave Systems Inc. Related Inventions cannot be separated from inventions produced under this Agreement, the parties and any Related Entities with an ownership right in such inventions agree to negotiate appropriate licenses for the continued use of D-Wave Systems Inc.'s Related Inventions.

(e) For Related Inventions owned by Caltech, Caltech agrees to consider and, if appropriate under the current Caltech policy, may grant D-Wave Systems Inc. a license to Related Inventions under mutually agreeable terms and conditions. Such terms and conditions shall be negotiated by the Caltech Office of Technology Transfer and D-Wave Systems Inc. pursuant to a separate agreement.

(f) The parties agree that the following inventions are Related Inventions which may be used in performance of this Agreement. This list may not be comprehensive and is subject to change during the course of work under this Agreement: **TBD**

(g) "Related Computer Software" means a Related Invention in the form of computer software. When Related Computer Software is provided by NASA or a NASA Related Entity to D-Wave Systems Inc., such software will be provided under a separate software license. D-Wave Systems Inc. agrees to maintain such Related Computer Software in confidence and use it only for carrying out D-Wave Systems Inc.'s responsibilities under this Agreement. Unless D-Wave Systems Inc. has entered into a license, consistent with 37 C.F.R. Part 404, for Related Computer Software provided under this Agreement, or entered into a commercial or government license agreement with Caltech for Related Computer Software owned or copyrighted by Caltech, upon completion of activities under this Agreement, all copies of such software will be disposed of as instructed by NASA.

(h) The parties agree that the following software is Related Computer Software which may be used in performance of this Agreement. This list may not be comprehensive and is subject to change during the course of work under this Agreement: **TBD**

ARTICLE 14. RELEASE OF GENERAL INFORMATION TO THE PUBLIC

NASA, D-Wave Systems Inc., or their Related Entities may, consistent with Federal law and this Agreement, release general information regarding their participation in this Agreement, as desired. D-Wave Systems Inc. agrees that all press releases resulting from activities conducted under this Agreement will be reviewed and approved by NASA Public Affairs prior to release. Such approval will be based on applicable law and NASA policy and will not be unreasonably withheld.

ARTICLE 15. USE OF NASA NAME AND NASA EMBLEMS

1. NASA Name and Initials:

D-Wave Systems Inc. agrees the words "National Aeronautics and Space Administration," the letters "NASA," or the name or mark of any NASA Related Entities will not be used in connection with a product or service in a manner reasonably calculated to convey any impression that such product or service has the authorization, support, sponsorship, or endorsement of NASA, or any NASA Related Entity, which does not, in fact, exist. D-Wave Systems Inc. agrees that any proposed public use of the NASA name or initials (including all promotional and advertising use) shall be submitted by D-Wave Systems Inc. in advance to the NASA Assistant Administrator for Public Affairs or designee ("NASA Public Affairs") for review and approval. Approval by NASA Public Affairs shall be based on applicable law and policy governing the use of the NASA name and initials. In addition, D-Wave Systems Inc. agrees that any proposed use of the name or marks of any NASA Related Entity (including all promotional and advertising use) shall be submitted by D-Wave Systems Inc. in advance to the NASA Related Entity Public Affairs Office or designee for review and approval.

2. NASA Emblems:

Use of NASA emblems/devices (i.e., NASA Seal, NASA Insignia, NASA Logotype, NASA Program Identifiers, and the NASA Flag) are governed by 14 C.F.R. Part 1221. D-Wave Systems Inc. agrees that any proposed use of such emblems/devices shall be submitted for review and approval in accordance with such regulations.

ARTICLE 16. DISCLAIMER OF WARRANTY

Equipment, Goods, Facilities, Technical Information, and Services provided by NASA or NASA Related Entities under this Agreement are provided "as is" and neither NASA nor its Related Entities make any express or implied warranty as to the condition of such Equipment, Goods, Facilities, Technical Information, or Services, or as to the condition of such Equipment, Goods, Facilities, Technical Information, or Services, or as to the condition of any Research, Information Generated, or Products made or developed under this Agreement, or as to the merchantability or fitness for a particular purpose of such Research, Information, or Resulting Product, or that the Equipment, Goods, Facilities, Technical Information, or Services provided will accomplish the intended purpose, or that any of the above will not interfere with privately owned rights of others. Neither the Government nor its contractors shall be liable for special, consequential, or incidental damages attributed to such Equipment, Goods, Facilities, Technical Information, or Services provided under this Agreement or such Research, Information, or Resulting Products made or developed under this Agreement.

ARTICLE 17. DISCLAIMER OF ENDORSEMENT

NASA does not endorse or sponsor any commercial product, service, or activity. NASA's participation in this Agreement and/or supply of goods (i.e., equipment, facilities, technical information, etc.) and services under this Agreement does not constitute endorsement by NASA. D-Wave Systems Inc. agrees that nothing in this Agreement will be construed to imply that NASA authorizes, supports, endorses, or sponsors any product or service of D-Wave Systems Inc. resulting from activities conducted under this Agreement, regardless of the fact that such product or service may employ NASA-developed technology.

ARTICLE 18. TERM OF AGREEMENT

This Agreement becomes effective upon the date of the last signature below and shall remain in effect until September 30, 2014.

ARTICLE 19. RIGHT TO TERMINATE

1. NASA's commitment under this Agreement to make available Government property and services required by D-Wave Systems Inc. may be terminated by NASA, in whole or in part, (a) upon a declaration of war by the Congress of the United States, (b) upon declaration of a

national emergency by the President of the United States, (c) upon D-Wave Systems Inc.'s failure to make payments as set forth in Article 6 (Financial Obligation), (d) upon D-Wave Systems Inc.'s failure to meet its obligations under the Agreement, or (e) upon a NASA determination, in writing, that NASA is required to terminate such services for reasons beyond its control. For purposes of this article, reasons beyond NASA's control are reasons which make impractical or impossible NASA's or its contractors' or subcontractors' performance of the Agreement. Such reasons include, but are not limited to, acts of God or of the public enemy, acts of the U.S. Government other than NASA, in either its sovereign or contractual capacity (to include failure of Congress to appropriate sufficient funding), fires, floods, epidemics, quarantine restrictions, strikes, freight embargoes, or unusually severe weather.

2. In the event of termination for reasons given above, NASA will seek to provide reasonable advance notice. D-Wave Systems Inc. will be liable for all costs, consistent with law and NASA policy, which are incurred by the U.S. Government in the provision of property and/or services, including termination costs associated with the Agreement activities.

3. NASA shall not be liable for any costs, loss of profits, revenues, or other direct, indirect, or consequential damages incurred by D-Wave Systems Inc., its subcontractors, subcontractors, or customers as a result of the termination by NASA pursuant to paragraph 1 of this article.

4. NASA and D-Wave Systems Inc. shall have the right to terminate, in whole or in part, this Agreement at any time. Such termination shall be effective 30 days after written notice from NASA or D-Wave Systems Inc. is received by other party. In the event of D-Wave Systems Inc.'s termination, D-Wave Systems Inc. will be obligated to reimburse NASA for all Government costs which have been incurred up to the effective date of D-Wave Systems Inc.'s notice of termination and are incurred as a result of such termination.

5. This article is not intended to limit or govern the right of NASA or D-Wave Systems Inc. in accordance with law, to terminate its performance under this Agreement, in whole or in part, for D-Wave Systems Inc. or NASA's breach of a provision in this Agreement.

ARTICLE 20. MISHAP INVESTIGATION

In the case of a mishap or mission failure, the parties agree to provide assistance to each other in the conduct of any investigation, bearing in mind, in particular, the provisions of Article 10 (Export Control). For all NASA mishaps, D-Wave Systems Inc. agrees to comply with NPR 8621.1, "NASA Procedural Requirements for Mishap Reporting, Investigating, and Recordkeeping."

ARTICLE 21. CONTINUING OBLIGATIONS

The obligations of the parties as set forth in the Articles entitled Liability and Risk of Loss, Intellectual Property and Data Rights (Articles 11, 12 and 13), and Financial Obligations (Article 6) shall continue to apply after the expiration or termination of this Agreement.

ARTICLE 22. KEY PERSONNEL

The following personnel are designated as the key officials for their respective party. The Technical Points of Contact are the principal points of contact between the parties in the performance of this Agreement. The business/administrative point of contact for NASA must be a NASA civil service employee.

Technical Points of Contact:

NASA

Dr. Alan Kleinsasser
NASA Jet Propulsion Laboratory
4800 Oak Grove Drive, Mail Stop 302-231
Pasadena, CA 91109
Phone: (818) 354-9186
Fax: (818) 393-4773
Email: Alan.W.Kleinsasser@jpl.nasa.gov

D-WAVE SYSTEMS INC.

Mr. Eric Ladizinsky
D-Wave Systems Inc.
100-4401 Still Creek Drive
Burnaby, BC, Canada V5C 6G9
Phone: (310) 971-7350
Fax: (604) 630-1434
Email: eric@dwavesys.com

Business/Administrative Points of Contact:

NASA

Mr. Raymond Wilkens, Contract Specialist
NASA Management Office – JPL
4800 Oak Grove Drive
Pasadena, CA 91109 USA
Phone: (818) 354-6069
Fax: (818) 354-6051
Email: Raymond.A.Wilkens@nasa.gov

D-WAVE SYSTEMS INC.

Mr. Warren Wall, Executive Vice President and Chief Operating Officer
100-4401 Still Creek Drive
Burnaby, BC, V5C 6G9 Canada
Phone: (604) 630-1428 ext. 416
Fax: (604) 630-1434
Email: wwall@dwavesys.com

ARTICLE 23. DISPUTE RESOLUTION

The NASA Key Personnel and D-Wave Systems Inc. Key Personnel set forth in the Agreement, or their successors, will attempt to resolve all issues arising from the implementation of this Agreement. If they are unable to come to agreement on any issue, then the dispute will be referred to a NASA Management Office Contracting Officer and one level higher of D-Wave Systems Inc.'s management, or their designated representatives, for joint resolution. If the parties are unable to resolve the dispute, the NASA Management Office Director will issue a written decision which shall be a final Agency decision for all purposes including judicial review.

ARTICLE 24. MODIFICATIONS/AMENDMENTS

Any modification to this Agreement shall be executed, in writing, and signed by an authorized representative of each party, possessing original or delegated authority to make such a commitment.

ARTICLE 25. ASSIGNMENT OF RIGHTS

Neither this Agreement nor any interest arising under it will be assigned by either party without the express written consent of the other party.

ARTICLE 26. ANTI-DEFICIENCY ACT

All activities under or pursuant to this Agreement are subject to the availability of appropriated funds, and no provision shall be interpreted to requite obligation or provision of funds in violation of the Anti-Deficiency Act, 31, U.S.C. 1341.

ARTICLE 27. APPLICABLE LAW

U.S. Federal law governs this agreement for all purposes, including, but not limited to, determining the validity of this Agreement, the meaning of its provisions, and the rights, obligations and remedies of the parties.

ARTICLE 28. SIGNATURE BLOCK

The signatories to this Agreement covenant and warrant that they have authority to execute this Agreement. By signing below, the undersigned agree to the above terms and conditions.

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION (NASA)

By: _____

Kent Bress
Director, Exploration Systems and
Aeronautics Research Division
Office of International and
Interagency Relations

Date: 22 June 2011

D-WAVE SYSTEMS INC.

By: _____

Warren Wall
Executive Vice President and
Chief Operating Officer

Date: 22 JUNE 2011

ADIABATIC QUANTUM COMPUTING FABRICATION PROCESS DEVELOPMENT

to

D-Wave Systems, Inc.
100-4401 Still Creek Drive
Burnaby, British Columbia V5C 6G9 Canada

JPL Task Plan No. 82-16404

JET PROPULSION LABORATORY
California Institute of Technology
Pasadena, California 91109

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ARTICLE 2. PURPOSE AND AGENCY COMMITMENT

A. INTRODUCTION

1. BACKGROUND

Advanced computer technology is critical to supporting JPL mission objectives. In particular, combinatorial optimization represents a problem class of central importance that pervades mission planning, engineering design, robotics and artificial intelligence. D-Wave Systems Inc. (hereinafter referred to as "D-Wave"), is developing Adiabatic Quantum Computing (AQC) as an approach to solving complex optimization problems by encoding data in arrays of Superconducting Quantum Interference Devices (SQUIDs) that act as quantum bits (qubits). The system remains in its ground state while adiabatically evolving from a simple, known configuration to a final configuration that provides the answer to the computational problem of interest. D-Wave has made numerous demonstrations of prototype AQC processors, which are projected to outperform conventional supercomputers by a wide margin within a handful of years.

JPL and D-Wave began a highly successful collaboration in 2005 under JPL Task Plan 82-10225, "Nb Quantum Computing" (Task Order NMO715801). The collaboration expanded in 2007 under the current JPL Task Plan 82-11375, "Nb Quantum Computing Circuit Fabrication" (Task Order NMO715967). The current Task Plan 82-11375 is scheduled to end on June 26, 2011. Both D-Wave and JPL desire to continue their successful collaboration through September 30, 2014 under this follow-on Task Plan, 82-16404. The nature and scope of the follow-on work described here are very similar to the work involved in the last two years of the current Task Plan 82-11375.

Beginning in 2005, the JPL Microdevices Lab (MDL) fabricated prototype circuits and processor chips for D-Wave, beginning with single devices and individual qubits. By late 2007, D-Wave was solving benchmark problems using a 28 qubit processor fabricated at JPL, enabling a critical experimental examination of the AQC approach and the beginning of scaling studies of computational power with the number of qubits in the array. In parallel, D-Wave and JPL developed classical superconducting circuitry to control the quantum circuits. In these collaborative efforts, JPL was the sole source of quantum hardware for D-Wave, handling process development, fabrication, and initial characterization while D-Wave handled circuit designs and functional testing.

By 2008, in anticipation of eventual commercial success and with technical support from JPL, D-Wave developed its own chip manufacturing capability. For the past several years, D-Wave has produced complex superconducting quantum processor chips with a distributed process based on SVTC, a commercial Complementary Metal Oxide Semiconductor (CMOS) circuit foundry in San Jose, CA. The availability of this process, arguably the most advanced superconductor process in the world, allows D-Wave to fabricate and yield 128-qubit chips containing approximately 25,000 Josephson junctions. These are the most complex superconducting chips currently being produced

anywhere. However, D-Wave must continue to advance its process in order to meet future goals that include demonstrating functional 512-qubit processors, each containing over 100,000 Josephson junctions, by the spring of 2012. Achieving these and future goals requires continuous process improvement. To that end, JPL remains an essential partner of D-Wave.

In any modern CMOS foundry, troubleshooting typical fabrication-related problems and introducing new materials and processes is costly and time-consuming. Fabricating superconductor circuits in such a facility introduces additional difficulties, as some essential materials and processes are non-standard. Although the benefits of operating a non-standard process in such a facility outweigh the costs, D-Wave's experience has taught that running, maintaining, and advancing its superconductor process requires close collaboration with an R&D facility operating in a rapid prototyping mode. This role has been filled by JPL, and D-Wave regards continued collaboration with JPL as essential to its success. This Task Plan defines for JPL a continuing R&D role that emphasizes support for D-Wave's manufacturing process development, rapid prototyping of advanced designs, new circuit approaches, and fundamental physical investigations.

2. JPL UNIQUENESS JUSTIFICATION

The Superconducting Materials and Devices Group in MDL has considerable, long-established expertise in the area of superconducting sensor fabrication, characterization, and application. In 2005, after visiting, and negotiating with corporate, academic, and government labs throughout the world having significant capabilities in the area of superconducting electronics, D-Wave concluded that JPL was, and is, uniquely qualified to meet its requirements. As a result, JPL and D-Wave have collaborated to develop AQC-related fabrication since mid-2005 and have an excellent, mutually beneficial relationship.

Over the past three years, D-Wave has established a fabrication capability based at the Silicon Valley Technology Center (SVTC), a commercial Research and Development (R&D) CMOS foundry. D-Wave boasts what is arguably the best superconductor process in the world. It features high throughput, high yield, and a complex vertical structure. JPL in no way competes with this industrial facility. Rather, JPL provides essential process development support. Some aspects of process development (e.g., introducing new materials) and troubleshooting of some process-related problems require an R&D facility operating in a rapid prototyping mode. This role has been filled by NASA/JPL, and D-Wave regards continued collaboration with NASA/JPL as essential to its success. In addition, JPL has specialty tools, including Molecular Beam Epitaxy (MBE) and Inductively-Coupled Plasma (ICP) Plasma Enhanced Chemical Vapor Deposition (PECVD), which are currently unavailable at SVTC but can be assessed for potential advantages. If such a process can be demonstrated to provide critical advantages, the lengthy process of establishing it at SVTC can be justified.

In collaborating with D-Wave, the JPL team has provided rapid turn-around Nb-based superconductor integrated circuit fabrication and characterization in close collaboration with D-Wave's manufacturing environment. JPL has no minimum lot size, in stark contrast to industrial organizations, which focus on throughput. JPL offers rapid turn-around of one-of-a-kind parts with a great deal of materials and process flexibility. It excels in developing new devices and process modules for insertion into a superconductor integrated circuit process. Specific JPL capabilities are listed in the following section. No industrial superconductor fabrication facility offers this set of capabilities.

3. JPL FACILITIES AND EQUIPMMENT

The JPL Superconducting Materials and Devices group has considerable experience in the design, fabrication, characterization and application of superconducting devices, routinely fabricating deep-sub μm Nb tunnel junctions, and circuits based on them. The MDL clean room facilities include a state of the art electron beam lithography facility, a sub-0.25 μm deep-uv stepper, and deposition and processing equipment for a wide range of metal and insulator deposition and etching processes. MDL also provides dc and radio frequency, electrical characterization facilities covering the full range from room temperature down to a few mK. In particular, MDL has an automated room temperature probe station and numerous cryogenic test facilities which are used to characterize the superconducting chips produced in this work.

Specific capabilities include:

- A Nb-based superconductor circuit process with up to 4 Nb wiring layers and no minimum lot size (important for rapid turn-around on "one-off" experiments).
- A well-established, low temperature fabrication process (<100 °C) that serves as a bench mark process against which the higher temperature processes in D-Wave's manufacturing environment (which includes >200 °C temperatures that that can degrade junction quality/spreads) can be compared (to understand and mitigate the effects of higher temperature)
- Deep-sub-μm device dimensions with deep-uv lithography.
- Direct-write e-beam lithography for dimensions below what is possible with optical techniques.
- Low temperature deposition (< 100 °C) of a wide range of high quality/low loss dielectrics (e.g., using ICP PECVD).
- Epitaxial/single crystal film growth that D-Wave values for its potential in combating noise in qubits.
- A wide variety of wet chemical etches for experimentation that are not readily available in a manufacturing environment
- The ability to readily incorporate or substitute novel materials (e.g., the superconductors NbTiN, TiN_x, and Al or dielectrics such as SiN_x and a-Si).
- The ability to incorporate alternative tunnel barrier materials (e.g., AlN_x via ECR or ICP plasma nitridation)) to produce more temperature resistant junctions.

- Characterization and testing from room temperature down to mK temperatures. A specific example of importance to D-Wave is mK characterization of dielectric loss-tangents (related to two level system noise that causes decoherence in qubits).

4. BENEFITS TO NASA/JPL

Combinatorial optimization is a foundational problem of central importance to JPL and NASA, pervading mission planning, engineering design, robotics, and AI. The AQC processors being developed by D-Wave can solve a wide range of combinatorial optimization problems. Future versions of the processors are expected to provide dramatic speed-up and improved solution quality. Thus, this collaboration opens the door to a broad spectrum of future AQC-related work at JPL.

In addition to supporting JPL and NASA interests in combinatorial optimization and quantum computing, this commercial collaboration both leverages and advances MDL superconducting sensor work in areas such as (1) Sub-μm superconducting tunnel junction fabrication in particular and superconducting circuit processing in general (e.g., sub-μm vias, high quality dielectric deposition, etching of oxides and metals, planarization, and increased circuit complexity). (2) Superconducting Quantum Interference Devices (SQUIDs). (3) Reduction of circuit noise at mK temperatures. (4) Ultralow temperature multiplexing/signal processing. This collaboration also supports key personnel and equipment and has provided significant support for MDL infrastructure

B. OBJECTIVE

The underlying goals of this Task Plan are the development of a fabrication process for Nb-based superconductor integrated circuits and its application to build Adiabatic Quantum Computers (AQC). In this Task Plan, JPL will test device and circuit concepts, perform R&D aimed at reducing circuit noise and decoherence, improve the efficiency of heat removal from operating chips, conduct fabrication process studies, implement fabrication process improvements, devise troubleshooting tests for process control, and develop methods to evaluate process effectiveness.

C. APPROACH

This Task Plan 82-16404 builds upon the past successful tasks and will include similar kinds of work. As described in the objective, JPL will test device and circuit concepts, perform R&D aimed at reducing circuit noise and decoherence, improve the efficiency

of heat removal from operating chips, conduct fabrication process studies, implement fabrication process improvements, devise troubleshooting tests for process control, and develop methods to evaluate process effectiveness.

JPL and D-Wave will be responsible for holding regular (bi-weekly to monthly) meetings to decide strategy and tactics. These meetings include discussion and evaluation of recent results, discussion and evaluation of near-term and long-term needs, and formulation of monthly and quarterly plans for collaborative activity, including specific plans for JPL activity. JPL will be responsible for delivering on the commitments included in these plans. As with the existing Task Plan, typical short-term commitments include fabrication at JPL of one or several wafers, characterization of their electrical properties, and delivery of test chips to D-Wave as required. Continuous communication between the parties is fundamentally important, and JPL will be responsible for providing, as needed, reports describing JPL fabrication and characterization activities, evaluation of process issues, and recommendations for future work.

Broad areas of JPL activity will include the following:

- Tests of device and circuit concepts. A successful example from the existing Task is the demonstration of a novel non-dissipative qubit readout scheme that has enabled dramatic speedup of future processor chips.
- Reduction of qubit and circuit noise/de-coherence. This work includes substitution of new superconductor or dielectric materials in parts of the process (or chip vertical structure), removal of unwanted oxides on existing wiring layers, and examination of the effect of processing on interfaces and sources of magnetic flux noise.
- Improvement of heat transfer from operating chips by substitution of new substrates and novel interface and substrate treatments. JPL will also consult on cryogenic thermal engineering of the cooling stages used for D-Wave devices and on methods to distribute heat at sub-Kelvin temperatures.
- Improving process yield through better understanding of, and controlling the effect of, oxidation temperature and small Al thickness variations on critical current density.
- Fabrication process improvements, including replacement AlO_x tunnel barriers by AlN ones, allowing significantly higher process temperatures, which will allow improved interlevel dielectric layers and better device parameter control.
- Fabrication process troubleshooting via short loop runs involving JPL processing of Josephson trilayers grown by D-Wave.
- Fabrication process evaluation via analysis of data provided by D-Wave and measurements on D-Wave samples.

The following specific activities are planned for the first year:

- Support the D-Wave fabrication process via short loop runs on sponsor-supplied wafers.
  - Nb wire deposition process

        - Determine T_c and resistivity uniformity and reproducibility
    - Josephson junction trilayer deposition process
        - Determine the effect on targeting and uniformity of film stress, Al thickness, gas purity and process temperature.
        - Monitor the effect on tunnel barrier resistivity of oxygen exposure and gas composition.
        - Determine the effect on vital device parameters of thermal annealing, with and without diffusion barrier layers at key locations in the vertical structure.
- Independent investigations at JPL
    - Compare techniques (wet chemical etching, ion milling, and plasma etching) for selective Nb oxide removal from wiring layers and employ Transmission Electron Microscope (TEM) cross sectional images to evaluate isotropy and selectivity.
    - Develop plasma-aided growth of high-quality AlN_x tunnel barriers to allow higher processing temperatures, ultimately providing a transferrable process with adequate uniformity, junction quality
    - SiN_x thin film deposition
        - Evaluate stochiometric, low temperature (<200 °C) PECVD Si_3N_4 deposition for junction hard masks and protective junction caps. Requirements include low stress, high uniformity, good adhesion to AlO_x, no resist poisoning.
        - Investigate resources for obtaining sputtered or PECVD SiN_x on 200 mm wafers. Requirements include good particle control, adequate throughput.
    - Reduce qubit body capacitance via air bridges and/or low k dielectrics.
- Collaborative process development
    - Investigations of qubit noise reduction will continue, with specific experiments to be defined based on testing by D-Wave of existing chips. These may include exploration of low temperature ICP PECVD deposition of SiO_2, SiN_x, and Si:H for interlayer dielectrics and SiN_x as a cap on wiring prior to SiO_2 deposition.
    - Experiments aimed at improving thermalization experiments will continue, with specific experiments to be defined based on testing by D-Wave of existing chips. These may include sapphire substrates, new bonding materials, and backside coatings.

- Collaborative device/circuit development
    - Evaluate, as circumstances dictate, novel circuit concepts by fabricating prototype wafers at JPL, with functional testing at D-Wave. Experiments may include study of schemes to introduce X-Z coupling to qubit interactions.
- Room temperature and cryogenic testing

- Obtain statistics on Nb film T_c, ΔT_c, p, RRR, λ measurements and compare JPL and D-Wave results to refine and improve measurement techniques and analysis.
- Develop understanding of the limits on correlating room temperature junction resistivity and low temperature critical current. Improve accuracy of extraction of I_c, R_n, V_g, ΔV_g, R_j/R_n from I-V data at 4 K and below
- Optimize the use of process-related data to improve process yields and collaborate with D-Wave to improve databases and their analysis.

D. INFORMATION REGARDING JPL AND NASA'S RELATIONSHIP

The Jet Propulsion Laboratory (JPL) is a government-owned contractor operated Federally Funded Research and Development Center (FFRDC) that conducts programs in Space Science and other scientific areas approved by its sponsor, NASA. JPL is operated for NASA by the California Institute of Technology (Caltech), which is a private educational institution.

Neither JPL nor Caltech is an arm of the Federal Government nor are any of their employee's agents of the Federal Government empowered to bind NASA to agreements with reimbursable sponsors.

Caltech operates JPL under NASA Contract NAS7-03001, which is administrated by Federal employees of the NASA Management Office located on-site at JPL. While Caltech is responsible for preparation of reimbursable proposals and performance of assigned tasks under the contract, agreements sending work to JPL are executed between Contracting Officers of the NASA Management Office, and the sponsor. Please be advised that Federal law places strict constraints on the types of work that an FFRDC, such as JPL, may perform for NASA or other sponsors.

All reimbursable work that NASA agrees to accept under NAS7-03001 must be consistent with its terms and conditions and JPL's mission as an FFRDC as determined by the NASA Contracting Officer in accordance with Clause C-1 (b) of the NAS7-03001.

E. SCOPE OF WORK

JPL will actively collaborate with D-Wave Systems Inc., to (a) develop, maintain, and improve a Nb-based superconductor circuit fabrication process that meets the requirements for producing quantum computing devices designed by the sponsor, and (b) characterize and maximize functionality of the resulting circuits.

In the performance of this work, JPL will, on a best-efforts, non-interference basis:

1. Support the D-Wave fabrication process via short loop wafer fabrication runs on sponsor-supplied wafers.
2. Investigate process and circuit performance improvements by applying unique MDL tools and processes to fabricate prototype circuits to be tested by JPL or D-Wave.
3. Evaluate, troubleshoot, and improve the D-Wave process by analyzing JPL and customer data.
4. Prepare technical progress reports as requested by D-Wave.
5. Prepare a follow-on Task Plan, if requested.
6. Prepare a Final Report.

ARTICLE 3. RESPONSIBILITIES

A. MANAGEMENT PLAN

As the JPL Task Manager, Dr. Alan Kleinsasser is responsible for the technical execution of this task, including cost, schedule, and performance. He is responsible for managing resources, coordinating the overall efforts, and accomplishing the formal deliverables identified in JPL Task Plan 82-16404. He will conduct weekly team meetings to assess team progress against the planned cost, schedule, and performance. In addition, Dr. Alan Kleinsasser must ensure that the costs remain within the allotted sponsor funding.

B. EXPORT COMPLIANCE

The technology described in this task plan Quantum Computing Circuit Fabrication is EAR 3E003. The JPL Task Manager will ensure compliance with export requirements.

ARTICLE 4. SCHEDULE AND MILESTONES

A. DELIVERY SCHEDULE

JPL will deliver to D-Wave Systems:

1. Superconducting test chips for D-Wave functional testing, as requested.
2. Informal technical progress reports (JPL format), as requested.
3. One copy of a follow-on Task Plan (JPL format), if requested before May 31, 2014.
4. One copy of a Final Report (JPL format), due on or before September 30, 2014.

ARTICLE 5. FINANCIAL OBLIGATIONS

A. COST ESTIMATE (dollars expressed in whole dollars)

Cost by Contractual/Programmatic

	Contractual			Programmatic			
	FY 2011	FY 2012 Oct-Mar	Contractual Total	FY 2012 Apr-Sep	FY 2013	FY 2014	Task Plan Total
1. Workhours							
JPL Hours	1,018	2,042	3,060	2,194	4,142	4,141	13,537
Cat A Hours							
2. Total Direct Compensation (includes Employee Benefits)	$86,121	$179,203	$265,324	$192,485	$378,047	$393,058	$1,228,914
3. Travel	$7,042	$1,434	$8,476	$5,782	$7,418	$0	$21,676
4. JPL Services	$20,250	$40,500	$60,750	$40,500	$81,000	$81,000	$263,250
5. Procurements							
Chargebacks	$5,496	$11,028	$16,524	$11,845	$22,369	$22,363	$73,101
Subcontracts							
Procurement RSA							
Purchases Orders	$9,000	$18,000	$27,000	$18,000	$36,000	$36,000	$117,000
Procurement IA							
Caltech Transfers							
6. Multi-Program Support	$13,343	$23,914	$37,257	$25,686	$49,875	$56,777	$169,594
7. Total Direct Costs	**$141,253**	**$274,079**	**$415,331**	**$294,298**	**$574,708**	**$589,197**	**$1,873,535**
8. Allocated Direct Charge	$47,030	$88,130	$135,161	$94,482	$178,161	$191,236	$599,039
9. Total JPL Costs	**$188,283**	**$362,209**	**$550,492**	**$388,780**	**$752,869**	**$780,433**	**$2,472,574**
10. NASA Costs	$6,360	$12,235	$18,595	$13,132	$25,431	$26,362	$83,519
11. Total Estimated Cost	**$194,643**	**$374,444**	**$569,087**	**$401,912**	**$778,300**	**$806,794**	**$2,556,093**

B. BASIS OF ESTIMATE

1. Labor

JPL in-house labor was estimated by the Task Manager and his supporting staff, and was based on a level of effort assessing specific proposed tasks. The proposed start date is July 2011 with a period of performance of thirty nine (39) months.

	Fiscal Year (Hours)				
Labor Category	**FY 2011**	**FY 2012**	**FY 2013**	**FY 2014**	**Total**
Engineering 3	521	2,169	2,122	2,121	6,933
Engineering 4	434	1,808	1,768	1,768	5,778
GS-Mgmt Time	43	179	175	175	572
STA	19	80	78	78	254
Total	**1,018**	**4,236**	**4,142**	**4,141**	**13,537**

2. Travel

Travel costs have been estimated to meet with Sponsor for Technical Inquiry Meetings (TIMs) and conference travel. JPL published rates were applied to determine such costs. (FY11_1_October 2011 rates) . San Jose rates were applied to carry out the TIMs held at such location. Washington, DC rates were applied to support the conference travel.

FY	Destination	Reason for trip	No. of Trips	No. of People	Duration	Airfare	Per Diem	Total
11	San Jose, CA	TIMs	2	2	2	$240	$230	$2,800
11	Cape Cod, MA	Conference	1	2	5	$506	$323	$4,242
							FY 2011 Subtotal	**$7,042**
12	San Jose, CA	TIMs	2	2	2	$249	$234	$2,868
12	Portland, OR	Conference	1	2	5	$524	$330	$4,348
							FY 2012 Subtotal	**$7,216**
13	San Jose, CA	TIMs	2	2	2	$257	$240	$2,948
13	TBD	Conference	1	2	5	$540	$339	$4,470
							FY 2013 Subtotal	**$7,418**
							Total	**$21,676**

3. Services

FY	Vendor	Description	Source	Total Amount
11	JPL-MDL	MDL Services - See attached quote for details	Quote	$20,250
			FY 2011 Subtotal	$20,250
12	JPL-MDL	MDL Services - See attached quote for details	Quote	$81,000
			FY 2012 Subtotal	$81,000
13	JPL-MDL	MDL Services - See attached quote for details	Quote	$81,000
			FY 2013 Subtotal	$81,000
14	JPL-MDL	MDL Services - See attached quote for details	Quote	$81,000
			FY 2014 Subtotal	$81,000
			Total	$263,250

4. Procurements

FY	Vendor	Description	Source	Total Amount
11	TBD-o Various vendors depending on availability	Consumables wafers, chemicals, tools, components, minor lab subtrates, targets, vacuum parts, masks, test equipment	Engineering estimate	$9,000
			FY 2011 Subtotal	$9,000
12	TBD-o Various vendors depending on availability	Consumables wafers, chemicals, tools, components, minor lab subtrates, targets, vacuum parts, masks, test equipment	Engineering estimate	$36,000
			FY 2012 Subtotal	$36,000
13	TBD-o Various vendors depending on availability	Consumables wafers, chemicals, tools, components, minor lab subtrates, targets, vacuum parts, masks, test equipment	Engineering estimate	$36,000
			FY 2013 Subtotal	$36,000
14	TBD-o Various vendors depending on availability	Consumables wafers, chemicals, tools, components, minor lab subtrates, targets, vacuum parts, masks, test equipment	Engineering estimate	$36,000
			FY 2014 Subtotal	$36,000
			Total	$117,000