Low Power Supercomputing in Space

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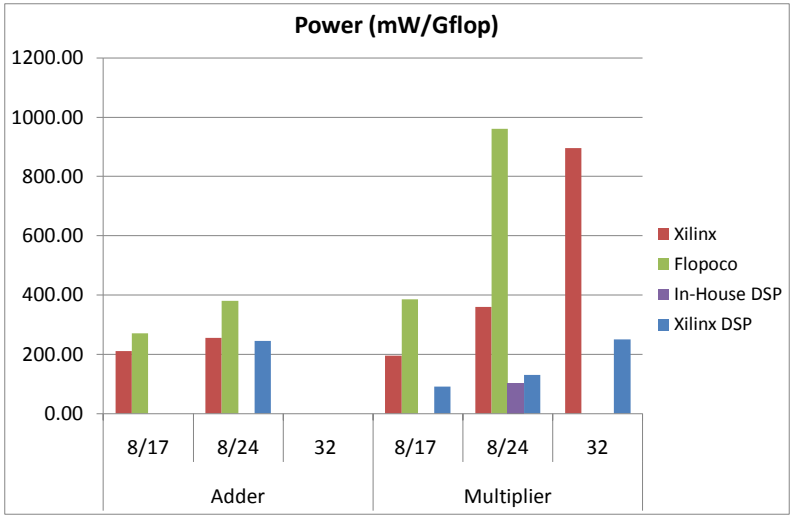
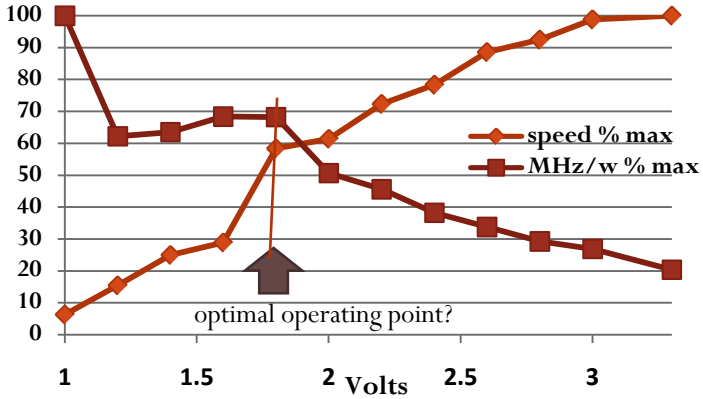
Technical Staff: Andrew J. Hartnett / JSC, Dave Rutishauser / JSC

NASA IPP
Summer 2010

- **Architecture**
  - High performance computing is usually either pipelined or multi-processor (aka multi-core)
    - *Reconfigurable FPGAs are now available with TeraFLOPs per chip*
    - *Energy per FLOP (floating point operation) much lower than in ordinary processor cores*
  - FPGAs considered hard to program
    - *Evaluated FPGA use for landing hazard detection (LiDAR data processing)*
    - *Development board with equivalent of newly available high capacity space FPGA financed by IPP funds*
- **Power**
  - Energy per operation decreases with voltage
  - Little known about radiation effects at low voltage
    - *Fabricated 90nm test chip and low power test rig with co-investigator*
    - *Heavy ion tests financed by IPP funds show unexpectedly good radiation performance*



Power efficiency of reconfigurable computing elements



Typical speed vs. power relation for CMOS

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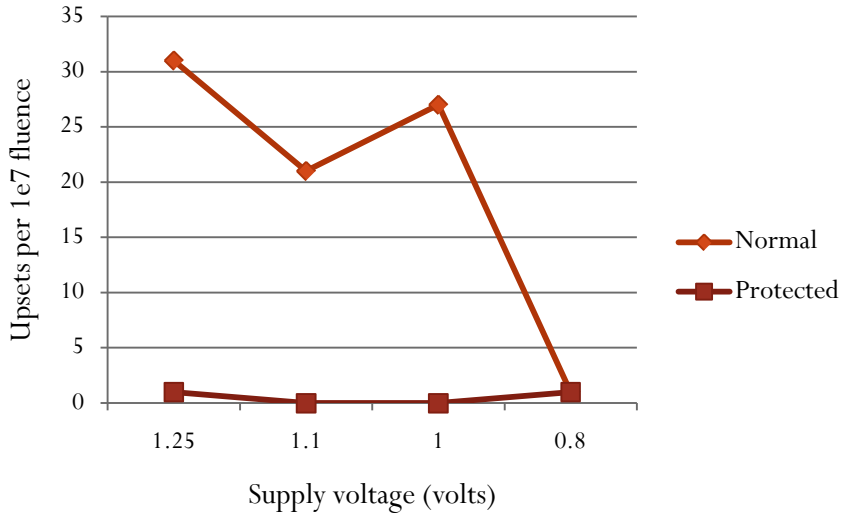
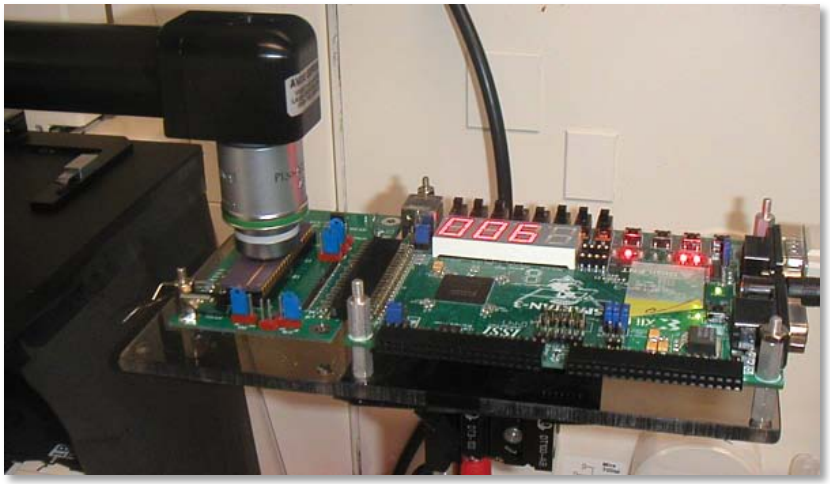
- **Low Power CMOS Radiation Testing**
  - Errors might have been expected to go up with decreasing voltage
  - What actually happened was…
    - *Little trend for radiation hardened by design circuits*
    - *Trend was down for normal circuits*
  - Conclusion – parallel low power circuits can be used in lieu of high power CPUs, radiation is a factor but not show stopper

Heavy ion testing at TAMU cyclotron facility





Laser testing at University of Saskatchewan

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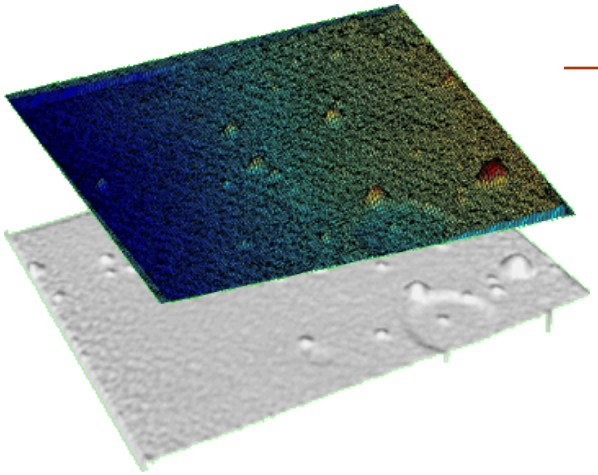
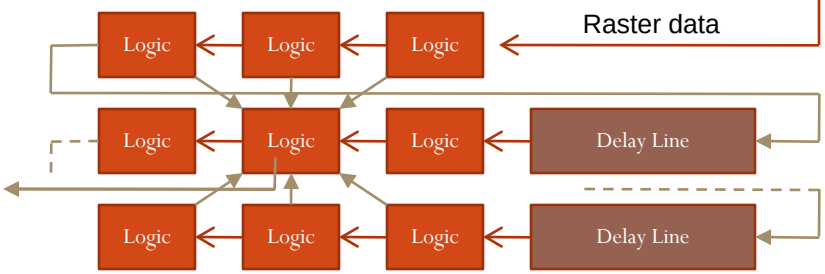
- **Landing Hazard Detection**
  - Coordinate conversion and re-gridding of LiDAR data complete
    - *Power on order of less than a watt*
    - *Plus chip overhead power 5-10 watts*
    - *Compare to multi-core ~30 watts*
  - Hazard detection expected to increase power only nominally, ~1 watt
    - *Requires improved programming methods*
- **Future Plans**
  - Development board purchased with IPP funds will be used to continue FPGA app studies
    - *Concept for application generator*
    - *Similar to signal processing app gen*
  - Funding will be sought for follow-on chip
    - *Fabrication of computational blocks*
    - *Possible application to hazard detection*



Digital Elevation Map generation (FPGA algorithm top)



Data flow framework for hazard application generator
2D computational scanning window of variable size and algorithm