NASA Technical Memorandum 86793

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March 1987

National Aeronautics and
Space Administration

NASA Technical Memorandum, 86793

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ABSTRACT

The highly integrated digital electronic control (HIDEC) program at NASA Ames Research Center, Dryden Flight Research Facility is a multiphase flight research program to quantify the benefits of promising integrated control systems. McDonnell Aircraft Company is the prime contractor, with United Technologies Pratt & Whitney, and Lear Siegler Incorporated as major subcontractors.

The NASA F-15A testbed aircraft was modified for the HIDEC program by installing a digital electronic flight control system (DEFCS) and replacing the standard F100 (Arab 3) engines with F100 engine model derivative (EMD) engines equipped with digital electronic engine controls (DEEC), and integrating the DEEC's and DEFCS. The modified aircraft provides the capability for testing many integrated control modes involving the flight controls, engine controls, and inlet controls.

This paper focuses on the first two phases of the HIDEC program, which are the digital flight control system/aircraft model identification (DEFCS/AMI) phase and the adaptive engine control system (ADECS) phase.

INTRODUCTION

Digital electronic controls in new aircraft enhance vehicle preformance by providing a means of integrating the flight and propulsion control systems. Substantial benefits are gained by exploiting the additional control devices available through digital controls on advanced design aircraft. These devices include symmetrical and differentially variable canards, variable leading- and trailing-edge flaps, variable geometry inlets, two-dimensional thrust vectoring and reversing nozzles, and other control variables associated with variable cycle engines. The complexity involved in the integration of these systems is governed by the digital logic. The integration of these systems enhances aircraft maneuverability, improves trajectory control for terrain following, terrain avoidance, and weapon delivery, and shortens takeoff and landing distances. Energy management techniques, when combined with trajectory control, can result in significant fuel and cost savings.

To develop and demonstrate integrated flight and propulsion technology, NASA Ames Research Center's Dryden Flight Research Facility initiated the highly integrated digital electronic control (HIDEC) program. McDonnell Aircraft Company (MCAIR) is the prime contractor, with Pratt & Whitney Aircraft (PWA) and Lear Siegler Incorporated (LSI) as major subcontractors. The test aircraft is an F-15, modified for installation of digital flight and engine control systems. The objectives of the program are to design, implement, and flight-test selected integrated flight/propulsion control modes which promise significant improvements in aircraft performance.

The HIDEC program is divided into five phases. These phases and the program schedule are shown in Fig. 1. Phase 1 of the HIDEC program involves the flight testing of the digital electronic flight control system (DEFCS) in the NASA F-15 airplane. The DEFCS consists of a higher-order-language digital flight control computer and two modified control augmentation system (CAS) analog computers used for sensor and actuator interface. As part of phase 1, the DEFCS software is programmed to provide a "flutter exciter" function that enables the pilot to select precise frequency sweep and dwell inputs to the horizontal tails. This feature allows the acquisition of data for improving the mathematical models of flight control components and aircraft rigid and structural modes.

Phase 2 of HIDEC, called the adaptive engine control system (ADECS, Ref. 1), consists of the design, implementation, and flight testing of an integrated flight and propulsion control mode. This mode uses flight control information to uptrim the engine pressure ratio for improved engine performance. Phase 3 of the program will consist of the development and evaluation of selected trajectory guidance algorithms. The algorithms will be tested with and without the ADECS features. Additional ADECS modes and enhancements to the basic features will be developed and tested during phase 4 of the HIDEC program. Phase 5 will involve efforts in the area of performance-seeking controls with the integration of the aircraft inlets to the engine and flight control systems. This paper concentrates on phases 1 and 2 of the HIDEC program, and includes discussions on the ADECS control system design, the computational architecture, the developmental testing, the built-in-test and in-flight integrity management system, and the plans for the flight tests included in these two phases.

Projections for engine performance improvements during the HIDEC program are contained in Ref. 1 and 2.

NOMENCLATURE

ADC	air data computer
ADECS	adaptive engine control system
AMI	aircraft model identification
AS	alternate shape, AMI excitation
A(ω)	amplitude, waveform frequency
BIT	built-in test
BUC	hydromechanical backup engine control
CAS	control augmentation system
CC	central computer
CID	Correction indicator display
CP	cockpit
DEEC	digital electronic engine control
DEFCS	digital electronic flight control system
DFCC	digital flight control computer
EMD	engine model derivative
EPR	engine pressure ratio
EPR_c	engine pressure ratio command
EPR_p	engine pressure ratio, predicted
FFT	fast Fourier transform
F_{lat}	lateral stick force
F_{long}	longitudinal stick force
FPR	fan pressure ratio
F_{rud}	rudder pedal force
FTIT	fan turbine inlet temperature
$FTIT_c$	fan turbine inlet temperature command
HIDEC	highly integrated digital electronic control
H009	data bus nomenclature
HUD	head-up display
IFIM	in-flight integrity management
INS	inertial navigation set
i	AMI command
LSI	Lear Siegler Incorporated
MCAIR	McDonnel Aircraft Company
MUX	multiplex
NCI	navigation control indicator
N1	engine fan speed
N1C2	engine fan speed, corrected to engine inlet conditions
$N1/\sqrt{\theta T_0}$	engine fan speed, corrected
n_y	lateral acceleration
n_z	normal acceleration
P	pitch CAS computer
PASCOT	programmable asynchronous serial communication translator
PCD	pitch CAS defeat
PLA	power lever angle
PSC	performance-seeking controls
PT2	fan inlet total pressure
PT2.5	fan discharge total pressure
PT6	turbine discharge total pressure
PWA	Pratt & Whitney Aircraft
p	roll rate
q	pitch rate
$\bar{q}$	pitch rate change
RF	radio frequency
RMDU	remote multiplex/demultiplex unit
R/Y	roll/yaw CAS computer
r	yaw rate
STF-FCL	software test facility-flight control lab
T_{amb}	ambient temperature
TH/ENG	throttle/engine
TRAJ	trajectory
t	time
UART	universal asynchronous receiver/transmitter data bus
V&V	verification and validation
W_{ac}	engine airflow, corrected
W_{AC2}	engine airflow, corrected to engine inlet
Wrap	wraparound software logic

α	angle of attack
α_p	angle of attack, predicted
β	angle of sideslip
β_p	angle of sideslip, predicted
δ_S	stabilator deflection
δ_R	rudder deflection
Δ	change
ω	frequency

AIRCRAFT DESCRIPTION

The test vehicle for this program is an F-15 airplane, modified with a digital electronic flight control system (DEFCS). The airplane is a high-performance, twin-engine fighter capable of speeds to Mach 2.5. The engine inlets are of the two-dimensional external compression type with three ramps, and feature variable capture area. The F-15 airplane is powered by two F100 engine model derivative (EMD) afterburning turbofan engines equipped with digital electronic engine controls (DEEC).

Digital Electronic Flight Control System

The DEFCS hardware consists of a four-channel digital flight control computer (DFCC) and two modified control augmentation system analog computers. The digital system features digital microprocessors for decreased volume and reduced cost, parallel processing architecture for increased throughput, and higher-order language for better programming efficiency and maintainability. The higher-order language currently used for the DFCC is PASCAL. Two channels in the DFCC contain the redundant pitch control laws, while the other two channels contain the redundant roll and yaw flight control laws. The modified analog computers provide the interface with the onboard sensors and actuators. The digital system emulates the analog F-15 control augmentation system (CAS) so that the handling qualities are identical to those of a standard F-15 airplane.

The avionics architecture is shown in Fig. 2. The programmable asynchronous serial communication translator (PASCOT) was installed in the aircraft to allow an interchange of information between the three multiplex buses: the aircraft standard H009 bus on which the central computer (CC) communicates with peripherals such as the inertial navigation system (INS) and the air data computer, the UART serial bus that transfers data from the DEEC engines (implemented during the ADECS phase), and the 1553A bus on which the DFCC and the instrumentation system communicate. The PASCOT permits both DEFCS and CC data to be sent to the onboard instrumentation system for recording, and for telemetering to ground receivers for real-time monitoring and postflight data processing.

The key features of the DEFCS are (1) the digital flight control computer, a Z8002 16-bit microprocessor with 490 kops and 26K memory, and four channels for communication; (2) MIL-STD-1553A multiplex interface; (3) PASCAL as the higher-order language; and (4) hardware that enables the system to be reconfigured as a triplex, quadruplex, or dual-dual system.

A significant feature for HIDEC is the higher-order-language compatibility which enables cost-effective programming of the DFCC for the subsequent HIDEC phases.

The execution of the DFCC executive program, input-output program, and flight control laws takes approximately one-half of the 12.5-msec duty cycle time and only about one quarter of the available memory. Thus there is ample cycle time and memory available to accomplish integrated control law calculations in the DFCC for the HIDEC phases.

Engine

The F100 EMD engine (Ref. 3) is an upgraded version of the F100-PW-100 engine that currently powers the production F-15 airplanes. The engine is built by Pratt & Whitney Aircraft and has a company designation of PW 1128. The engine incorporates a redesigned fan, revised compressor and combustor, single crystal turbine blades and vanes, a 16-segment augmentor with light-off detector, and a DEEC.

The DEEC is a full-authority digital control with an integral hydromechanical backup control. The DEEC controls the gas generator and augmentor fuel flows, the compressor bleeds, the variable inlet guide vanes, the variable stators, and the variable exhaust nozzle. It incorporates logic that provides closed-loop control of engine airflow and engine pressure ratio (EPR), limits the fan turbine inlet temperature (FTIT), and is capable of accepting inputs from the airplane and the many engine sensors. More detailed information on the DEEC is given in Ref. 4.

HIDEC PHILOSOPHY

The primary objective of the HIDEC program is to demonstrate and evaluate the improvements in performance and mission effectiveness resulting from engine/airframe control integration. The approach was to implement integrated engine/airframe control modes on the F-15 airplane, concentrating on the areas of adaptive engine control system modes and trajectory guidance modes. A key element of the HIDEC program philosophy was to provide a cost-effective demonstration of integrated controls technology. This meant constructing a technology demonstrator aircraft on which the latest digital technologies could be implemented and evaluated efficiently. Implementation of the proposed control modes was achieved in a cost-effective manner through the use of technologies developed for the digital flight control system and digital engine controls. The digital implementation provides both a direct interface with other digital avionics systems and the computational capability required to flight test integrated flight and propulsion control modes.

Another key element in the HIDEC program philosophy was the reduction of past social prejudices, thus allowing the demonstration of more complex control system integration between the airframe and propulsion components. The prejudices are based on the reluctance to implement major engine control modes in the aircraft computers. The major components of the HIDEC system are existing hardware ("hardware of convenience") that contain a limited redundancy level. Therefore, the architecture and system operation are based on a "fail-off/fail-safe" philosophy. This means that in case of major failures of the HIDEC modes or hardware, the operating system would revert to the standard aircraft (non-HIDEC) modes or the basic mechanical systems.

For the HIDEC program, critical engine control parameters, such as engine pressure ratio, are commanded from the flight control computer. In later phases, additional engine parameters such as airflow and fan turbine inlet temperature also will be commanded from the flight control computer. The logic for generating these commands is programmed in a dual redundant fail-off manner in the flight control computers. In the failed situation, the engine returns to standard DEEC control operation. The DEEC itself contains protection from excessive commands that could result from a flight control computer failure or from interface wiring failures. The successful testing of the HIDEC/ADECS phase will reinforce the significant performance gains that can be realized with the more complex control system integrations without the extensive redundancy levels.

HIDEC TEST PHASES

The current HIDEC program consists of five test phases. Phase 1 of the program concentrated primarily on the installation and evaluation of the digital flight control system in the F-15 airplane and an aircraft model identification (AMI) flight test series. Phase 2 involves the development and flight test of the adaptive engine control system (ADECS) modes. The development, implementation, and flight test of the trajectory guidance control laws and associated aircraft modifications are primary in phase 3 of the HIDEC program. Phase 4 involves the development and flight test of enhanced ADECS modes, coupled with the trajectory guidance work from phase 3. Performance-seeking controls development and flight test evaluation constitute phase 5 of the program. During the course of the various program phases, the F-15 airplane and supporting systems will be modified into a facility testbed available for other integration-type experiments and related developmental activities. The remainder of this paper will concentrate on the activities involved in phases 1 and 2 of the program.

Phase I - Digital Electronic Flight Control System/Aircraft Model Identification (DEFCS/AMI)

Digital electronic flight control system. The DEFCS flight test phase verified the operation of the digital flight control system in the NASA F-15 airplane and expanded the DEFCS flight envelope to that required for the HIDEC program. The DEFCS system had previously flown under a McDonnell Aircraft Company (MCAIR) research and development program, with additional flight evaluations performed in a cooperative effort between the Air Force and MCAIR. The test phase consisted of pilot evaluations of the airplane and data analysis that compared the DEFCS operation with the analog CAS.

The NASA F-15 airplane was flown with the DEFCS during February and March 1985. On six dedicated flights flown by three different NASA test pilots, the DEFCS was tested throughout the current F-15 envelope. The test maneuvers designed to thoroughly check aircraft flying qualities were formation flying, touch-and-go and single engine waveoffs. Unanimous pilot opinion concluded that the F-15 aircraft handling qualities with DEFCS installed were the same as an F-15 with the standard analog control augmentation system (CAS), with the exception that roll response and formation flying were somewhat improved relative to using the analog CAS.

Aircraft model identification. One of the main concerns in the design of advanced aircraft is that of accurately modeling the aircraft rigid body and structural modes, and flight contol components (actuators, sensors). In the design of control systems for statically unstable aircraft, the area of actuator and structural mode modeling accuracy is crucial.

The most desirable method of constructing and verifying math models is to compare the model response with that obtained in flight. This was done previously by equipping an aircraft with "flutter exciter" hardware, obtaining flight test data, and reducing it by using fast Fourier transform (FFT) techniques to obtain frequency responses of aircraft and actuator performance. This flutter exciter hardware is typically quite expensive because it must be custom designed for each particular aircraft installation. Also, once designed and installed, the hardware has very limited flexibility in changing the type of excitation. Conversely, incorporation of a flutter exciter function in the flight control system software is relatively inexpensive because no additional hardware is needed. It is also very flexible because additional types of excitations can be programmed easily.

For the preceding reasons, the HIDEC program extended the DEFCS phase 1 testing to include the aircraft model identification (AMI) tests. These tests demonstrated the concept of obtaining ground and flight test data for improved modeling accuracy by adding a software module to the digital flight control computer. The method used for the AMI flight tests is summarized in Fig. 3. The AMI method is functionally similar to flutter exciters implemented previously in hardware on the F-15 and F-18 airplanes. For the HIDEC/AMI application, sinusoidal commands are issued to the collective horizontal stabilators. As indicated in Fig. 3, the AMI exciter module is one of several DFCC modules containing the menu select logic, the fade-in circuitry, limiters, and an automatic disengage function. The resulting AMI excitation is input to the flight control laws immediately before issuing a stabilator deflection command to the stabilator series servos.

Figure 4 shows the HIDEC/AMI crew station configuration. A control panel was added to select the AMI mode and to defeat the pitch CAS when desired. Two destination locations in the standard F-15 navigation control indicator (NCI) are used for entering AMI data, such as the frequency range for the excitation sweep, sweep rate, and amplitude of the sweep (which can be frequency dependent). An upfront panel was added to show the pilot when the system was operating or in the reset mode, whether the previous excitation was terminated abnormally, and which AMI modes were selected (such as pitch, CAS defeat, and alternate excitation shapes). Following proper AMI mode setup, the pilot must depress the couple button on the throttle to cause the excitation signal to be sent to the stabilator. The paddle switch on the stick can be used as an emergency disengage if the pilot encounters a problem during the AMI test.

The flight testing of the AMI modes includes a range of Mach numbers from 0.2 to 1.2 and altitudes from 5,000 to 30,000 ft. The F-15 test aircraft is extensively instrumented to gather all pertinent aircraft motion, surface deflection, and actuator input-output information. The NASA ground station is capable of performing "real-time" FFT's which can be calculated in about 30 seconds following a frequency sweep test. The FFT's are used on selected sweeps to verify that good data is being generated during a particular test point, and that no undetected problems exist.

The principal data reduction is done post-flight using flight data tapes and real-time information from the flight. The results from the flight test data are used to illustrate the capability of improving math models of the aircraft and its flight control components using the AMI technique.

PHASE 2 - Adaptive Engine Control System (ADECS)

The HIDEC/ADECS phase is designed to demonstrate improved engine performance using flight control information which has not been previously available for engine control operation. Information exchange is facilitated by the use of digital systems on the airplane – the DEFCS for flight control, and the DEEC for engine control. In the ADECS uptrim mode, additional thrust is obtained at intermediate and higher power settings by decreasing the nozzle throat area to increase engine pressure ratio. Increased engine pressure ratio results in increased engine thrust.

ADECS modes. A typical fan map in Fig. 5, illustrates what happens during subsonic uptrim. Fan pressure ratio (FPR) and engine pressure ratio (EPR) are related, differing only in the bypass duct pressure losses. Thrust is increased by increasing EPR along a constant, corrected fan speed line. This is accomplished with little reduction in engine airflow. Because higher fan turbine inlet temperatures (FTIT) are required, for the initial ADECS tests this mode is used only when the engine is not on the FTIT limit. Uptrim is allowed until the normal maximum FTIT limit is reached, then the uptrim is held constant along the FTIT limit to prevent reduction in engine life, which results from the engine being operated above the FTIT limit.

When EPR is uptrimmed, increased thrust is obtained at the expense of reduced engine stall margin. Significant stall margin is normally built into the engine control schedules. A large part of this margin is designed to accommodate inlet distortion produced at high angles of attack or sideslip. In the ADECS mode, some of the stall margin reserved for inlet distortion is used to increase thrust in regions of low distortion. When the inlet distortion is high, EPR is reduced and stall margins are restored. For more information on the stability audits and definition of the amount of stall margin available, see Refs. 1 and 2.

Subsonic uptrim is implemented as shown in Fig. 6. The necessary control laws are incorporated into the digital flight control computer. When predicted angle of attack and sideslip angles are moderate, the controller issues an EPR command to the engine, causing the engine to operate closer to the stall line. The controller senses airframe pitch, roll and yaw rates, and accelerations to predict angle of attack and sideslip angles in the immediate future. When these predicted angles become large, the controller will immediately wash out the uptrim signal in a well-behaved transient without stalling the engine.

The details of the ADECS EPR uptrim logic to be implemented in the DFCC are described in Ref. 2. The EPR uptrim is based on the minimum of the maximum amount of EPR allowable, for increased performance and the maximum amount of EPR allowable for engine stall considerations. Implementing this control law requires both airframe information (angle of attack, sideslip, and Mach number) and engine data (airflow, fan speed, and pressures at the engine face).

ADECS modes implementation. The HIDEC architecture used for the ADECS modes is shown in Fig. 7. The PASCOT has additional capability as a multiplex bus controller unit to transfer the information flow among the aircraft sensors (H009 bus), to the digital flight control computer (1553 bus), and the digital electronic engine controller (serial databus). The PASCOT also acts as an interface unit for the HIDEC control panels.

Figure 8 details the ADECS implementation, including where the ADECS control laws and in-flight integrity management software reside, and gives the data rates for communication among the key ADECS system computers. The ADECS control laws are computed in both the pitch A and B channels within the DFCC when both the HIDEC and ADECS modes are selected. The built-in test (BIT), in-flight-integrity management (IFIM) test, and related safety tests for the ADECS modes are also executed in this manner. Commands are then issued from the DFCC through the PASCOT to the DEEC.

The airplane crew station configuration for this phase is shown in Fig. 9. The HIDEC control panel is used to activate the HIDEC modes, to

select the engine(s) – left, right, or both – to receive the ADECS command(s), and to select the ADECS mode and the submodes (EPR, or a combination of EPR and FTIT) for a particular test sequence. Data entry locations through the NCI Panel are provided to initiate BIT's and to enter revised ADECS data for use in the DFCC. There are four destination entries in the NCI converted to select revised ADECS parameter data from stored values in the DFCC, providing great flexibility for the flight test experiments.

The upfront panel displays ADECS system coupling, IFIM failure, and automatic commands destination(s) – to the engine control (TH/ENG), or to the flight control system, or to both. The couple command button is on the throttle lever and the emergency disconnect for the system is through the paddle switch on the control stick.

ADECS verification and validation process. The ADECS phase of the HIDEC program entails software additions and modifications to both the airframe computers (digital flight control computer and central computer) and to the DEEC computer. The modifications to these systems were thoroughly verified and validated prior to flight. This section describes the key elements of the verification and validation (V&V) process before installation of the equipment on the aircraft. It also describes the built-in test (BIT) and in-flight-integrity management (IFIM) features for installed monitoring and checkout of the HIDEC system operation.

The DFCC, CC, and DEEC computers all undergo individual module testing and module integration tests. These verify that the code is programmed correctly to compute the appropriate variables and logic, and that all interfaces between modules are correct. The modual testing establishes the memory and throughput (duty cycle time) requirements for each computer.

The next step in the V&V process is the HIDEC system integration testing. The DEEC controllers are tested with the PASCOT multiplex bus control unit to verify the proper interfaces so that the aircraft computer (DFCC) can exchange information with and issue commands to the DEEC's. The remainder of the HIDEC equipment is tested as a system at the MCAIR software test facility-flight control lab (STF-FCL). The test configuration is illustrated in Fig. 10 and includes the DFCC, CC, PASCOT, control panels, and NCI. Models of the aircraft, atmosphere, engine, DEEC, and inlets reside in the host HARRIS computer. The objectives of this integration test are as follows:

1. validate CC, PASCOT, DFCC, indicator lights and control panel interfaces,
2. validate 1553 & H009 mux bus operation,
3. validate use of the NCI to
   a. select different gains
   b. read memory locations
   c. perform diagnostic maintenance functions
   d. select ground test mode
   e. select avionic preflight BIT
   f. display failed preflight test number,
4. validate the
   a. ADECS control laws
   b. safety features
   c. couple/uncouple criteria,
5. resolve any throughput timing problems.

The integration testing identifies and eliminates most of the HIDEC system interface problems.

The MCAIR manned simulation facility is used as part of the V&V testing following the integration testing in the STF/FCL. The manned simulation facility provides a 20-ft dome for scenic projections and a higher fidelity simulation with a simulated F-15 crew station. The major HIDEC hardware components (DFCC, CAS computers, PASCOT, CC, NCI, and HIDEC panels) are included in the manned simulation tests for a final certification of the HIDEC system before delivery to the aircraft. The HIDEC manned simulation testing diagram is shown in Fig. 11. The CYBER computer connected with the facility allows higher fidelity models of the aircraft, aircraft sensors, engine, DEEC, and inlets to be used than was possible in the STF-FCL simulation. The objectives of the manned hardware-in-the-loop simulation are as follows:

1. verify proper operation of the ADECS control laws under realistic pilot inputs throughout flight envelope,
2. verify proper operation and suitability of ADECS safety features,
3. familiarize the pilot with the ADECS control functions,
4. assess ADECS performance benefits.

Testing in the manned simulation facility is the final step in the V&V process before delivery of the hardware to the aircraft. At the close of these tests the software is "frozen" in its configuration. Any changes to the flight-critical software after completion of the manned simulation tests may require a retest in the manned simulation facility for certification.

ADECS ground test, maintenance functions, and built-in-tests. Once the HIDEC equipment is installed on the aircraft, tests must be performed to determine if it is functioning properly. The tests are required for checkout following equipment installation or some system anomaly, and as an automatic preflight test.

To satisfy the need for the manually run tests following initial installation, a ground test function and a maintenance function are incorporated in the HIDEC system DFCC and CC software. The ground test function allows the ADECS software to be operated on the ground and EPR uptrim signals sent to the DEEC. The proper functioning of the HIDEC system can be assessed by monitoring system variables using mux monitors and instrumentation system outputs. Using the NCI panel keyboard and display, the maintenance function allows access to CC and DFCC selected memory locations for altering them and reading data from the DFCC and CC for troubleshooting. For the ADECS flight

phase, this function also allows various parameters and schedules to be selected, and access to the DFCC and CC for verification of the software version and checksums.

The built-in tests can be initiated before each test flight to automatically check the following: PASCOT-initiated BIT, DFCC/PASCOT/CC MUX interface, DFCC power-up BIT, ADC validity, INS validity, DFCC/PASCOT/DEEC MUX interface, and DEEC power-up BIT.

ADECS in-flight integrity management/coupling criteria. The HIDEC system, in the ADECS mode, must pass an extensive set of IFIM tests and coupling criteria before allowing commands to pass from the aircraft DFCC to the (DEEC). The IFIM tests and coupling criteria logic are active whenever the HIDEC system is on and the modes are coupled. The following IFIM checks must be passed before allowing coupling between the DFCC and DEEC:

1. DEFCS self checks,
2. Central computer self checks,
3. H009 multiplex bus checks,
4. PASCOT self checks,
5. 1553 multiplex bus checks,
6. DEEC self checks
   a. critical failure indications
   b. fault indicators,
7. Wraparound cross checks
   a. DFCC/PASCOT/CC
   b. DFCC/PASCOT/DEEC/CC

To allow coupling between the DFCC and DEEC for the ADECS modes, the following criteria must be met:

1. correct control panel switches are initiated,
2. more than one second has passed after switch initiation,
3. throttle couple button is depressed each time ADECS mode couple is desired,
4. no HIDEC system IFIM faults are indicated,
5. no aircraft system faults are indicated,
6. aircraft angle of attack is within specified limits,
7. landing-gear-up discrete is present (or simulated),
8. wraparound multiplex channels are operating.

The checks are verified as operational during the ground tests on the aircraft following HIDEC equipment installation. Certain subsets of these tests are checked before each flight using the built-in test function described earlier.

ADECS flights. The flight test consists of both 1 g accelerations, and selected flight test maneuvers for evaluating the system between 10,000 and 40,000 ft altitudes at speeds ranging between Mach 0.3 and 2.0. More detailed information regarding the predicted performance of the HIDEC modes is in Refs. 1 and 2.

Future plans for the HIDEC program involve research in the area of trajectory guidance. The further development and evaluation of selected guidance algorithms, such as optimal guidance, optimal interception, energy management (minimum time/minimum fuel), and maneuver autopilot techniques will aid in the evaluation of the ADECS modes. The algorithms will be evaluated in the manual mode and automatic mode, with and without the ADECS modes, and will provide additional information on the benefits of engine/airframe integration technology. The HIDEC F-15 aircraft will provide a test facility for developing and evaluating the trajectory guidance algorithms using a ground-based computer and sending the command information to the aircraft, with the potential of transferring the final algorithms to an onboard auxiliary airborne computer. Performance-seeking controls and advanced ADECS modes to be developed are discussed in Ref. 1.

CONCLUDING REMARKS

The objective of the HIDEC program is to demonstrate and evaluate the improvements in performance and mission effectiveness resulting from engine/airframe control integration. The approach uses the technologies being developed in the areas of digital flight control systems and digital engine controls to implement integrated engine/airframe control modes. The program philosophy and course of action have been successful in developing an integrated engine/airframe test program in a cost-effective manner.

Phase 1 testing of the digital flight control system developed the basic HIDEC architecture and evaluated the operation of the DEFCS in the NASA F-15 airplane. The tests were successful, with no major differences noted between the digital flight control system and the standard F-15 analog CAS system. The aircraft model identification flight tests provide airframe aeroservoelastic flight data to compare with math models by using a "software excitation system" to excite the airplane structural modes.

Phase 2 testing concentrates on the ADECS control modes. The development of the control modes and logic demonstrates the integration necessary between the airframe and propulsion systems. The verification and validation process involves individual module testing, module integration testing, and hardware bench integration tests culminating in the manned hardware-in-the-loop simulation tests. The BIT and IFIM features provide a means of checking the integrity of the various HIDEC systems both on the ground and in flight, before and during HIDEC mode operations. Final validation of the HIDEC systems is performed during the aircraft ground tests, to be followed by the flight tests.

The NASA F-15 aircraft is being developed as a national facility "test-bed" for flight and propulsion integration and related experiments. The architecture and techniques developed during the HIDEC program will provide the flexibility to allow generic research to be conducted in the engine/airframe integration technology area.

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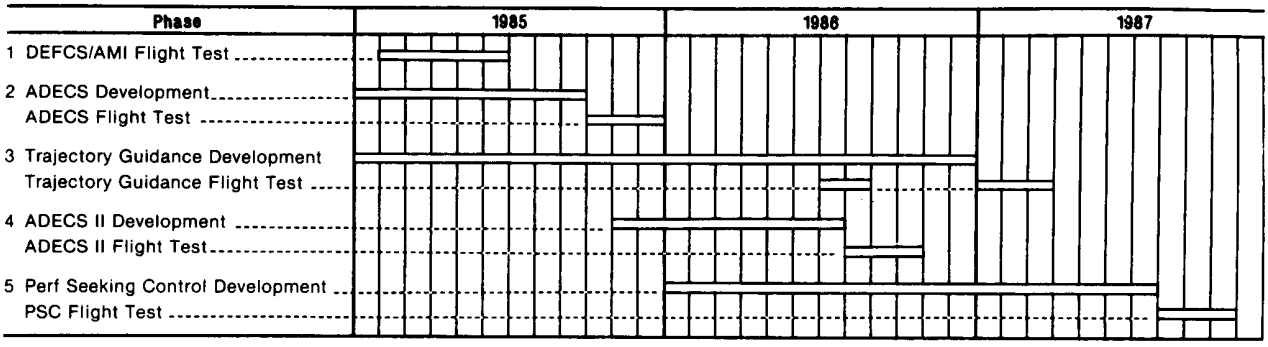

Fig. 1. HIDEC program schedule.

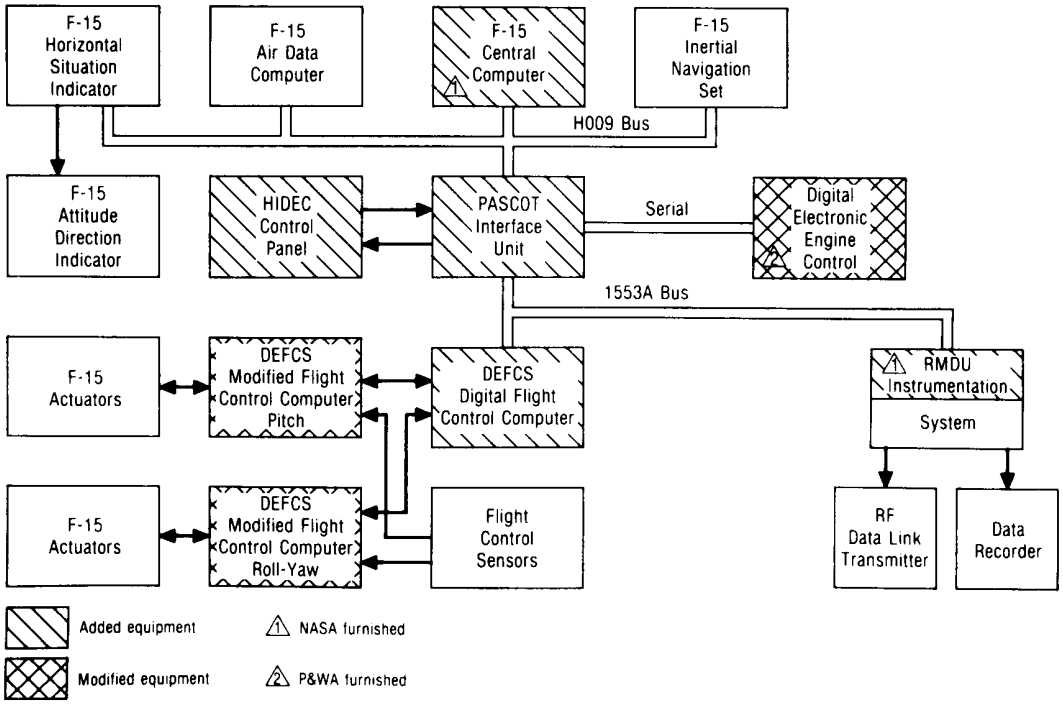

Fig. 2. HIDEC ADECS avionics architecture.

- SOFTWARE AMI EXCITER IN DFCC
  - FUNCTIONALLY SIMILAR TO EXISTING F-15 AND F/A-18 HARDWARE FLUTTER EXCITERS
  - PITCH AXIS ONLY (COLLECTIVE STABILATORS)
  - FREQUENCY SWEEP AND DWELL TESTS CONTROLLED BY PILOT (0.5 TO 20 Hz)

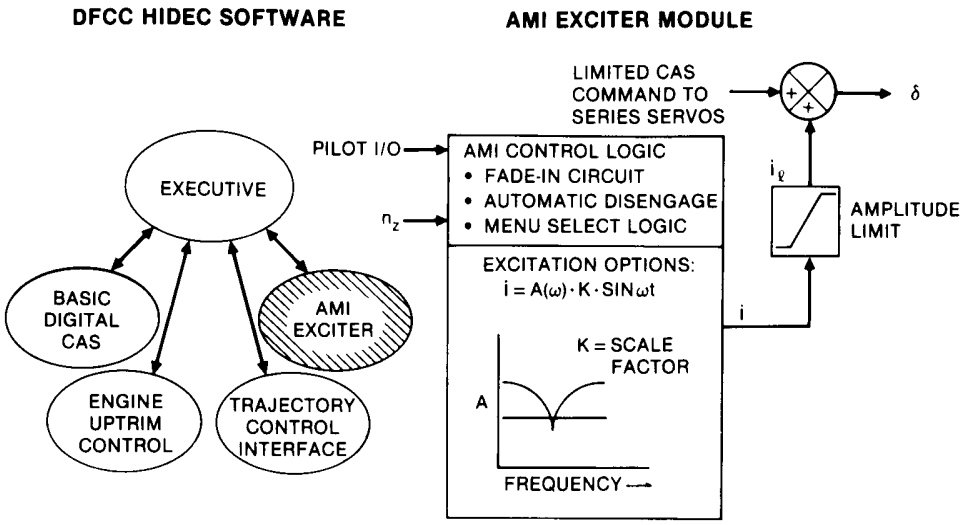

Fig. 3. Aircraft model identification.

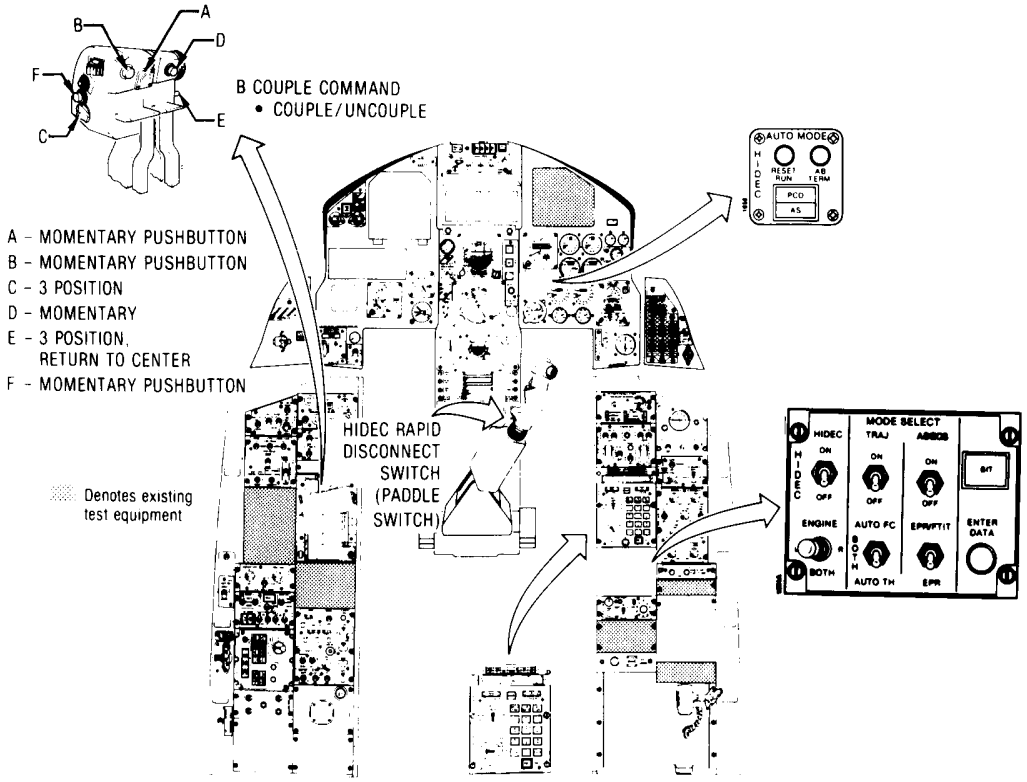

Fig. 4. HIDEC/AMI crew station orientation.

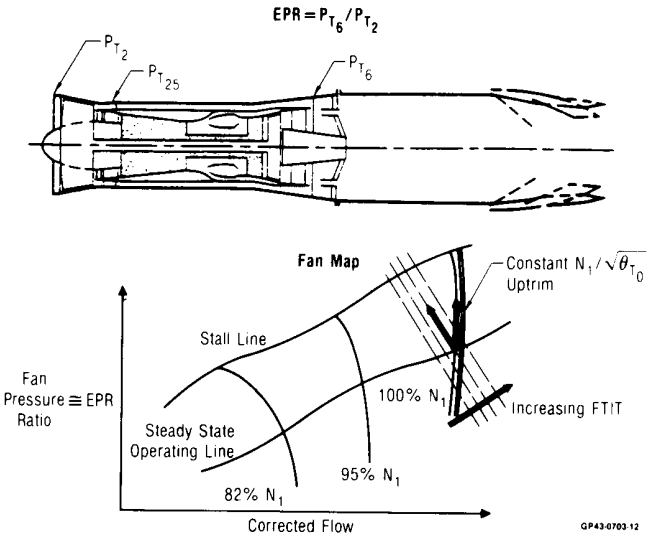

Fig. 5. Adaptive engine control system, subsonic uptrim.

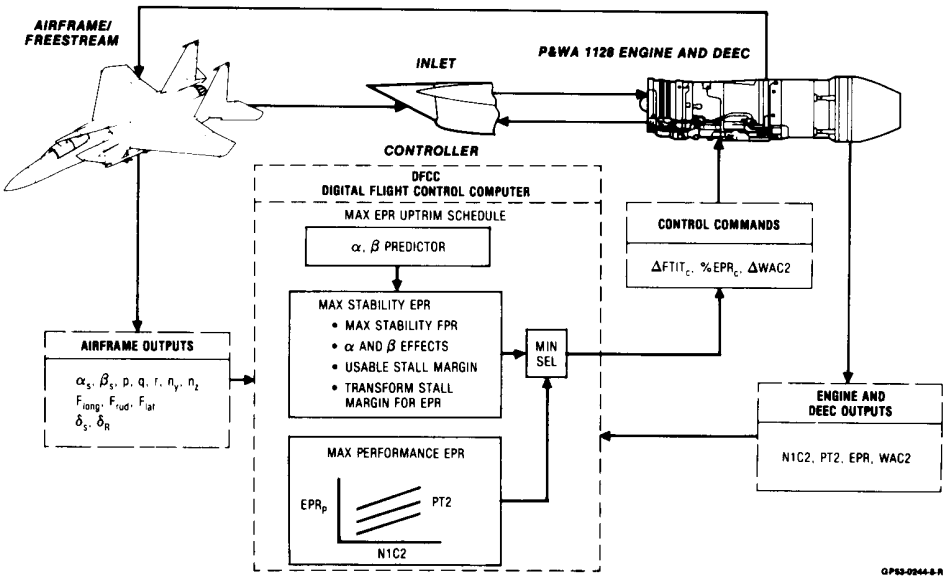

Fig. 6. Adaptive engine control system, subsonic EPR uptrim.

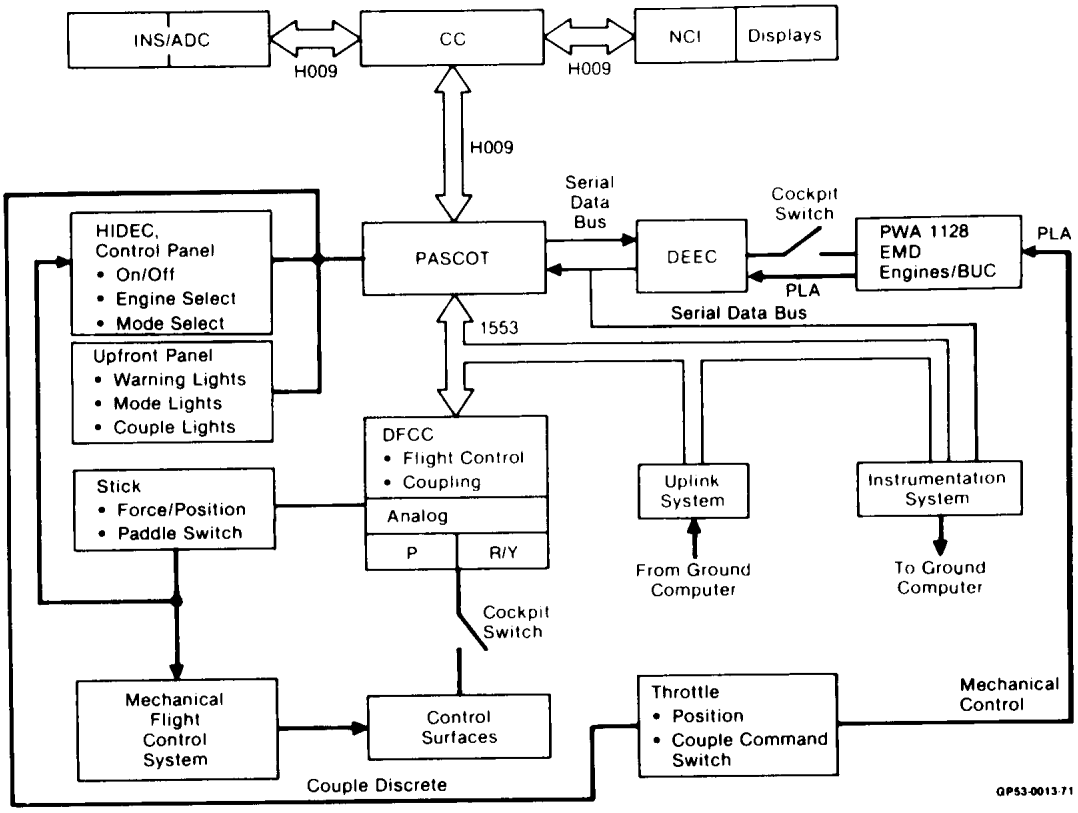

Fig. 7. HIDEC system architecture, ADECS modes.

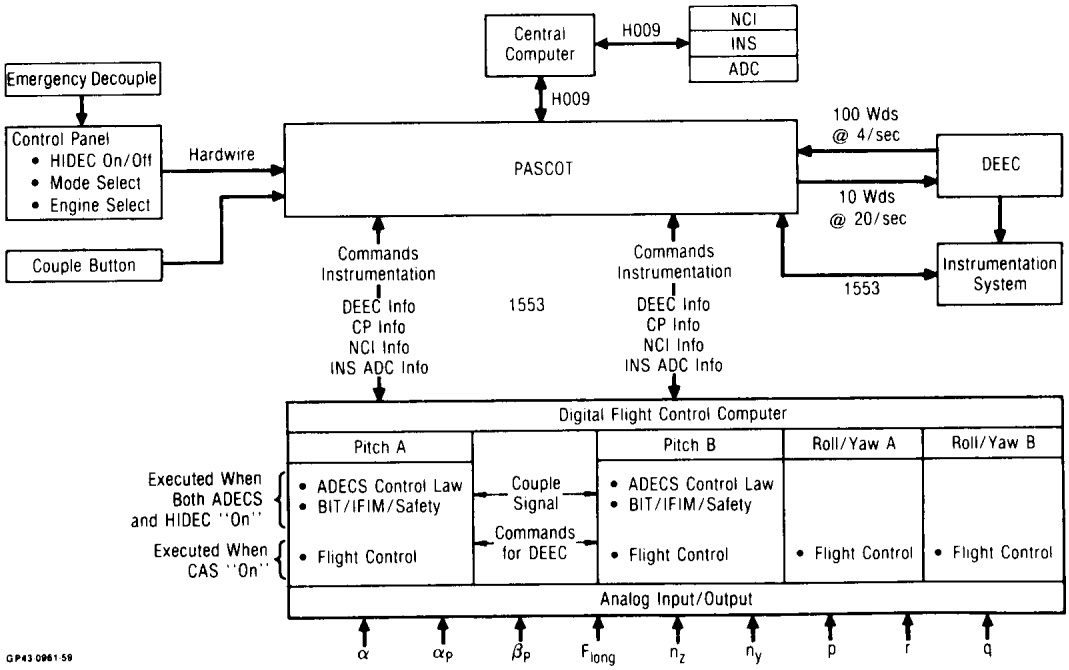

Fig. 8. ADECS architecture.

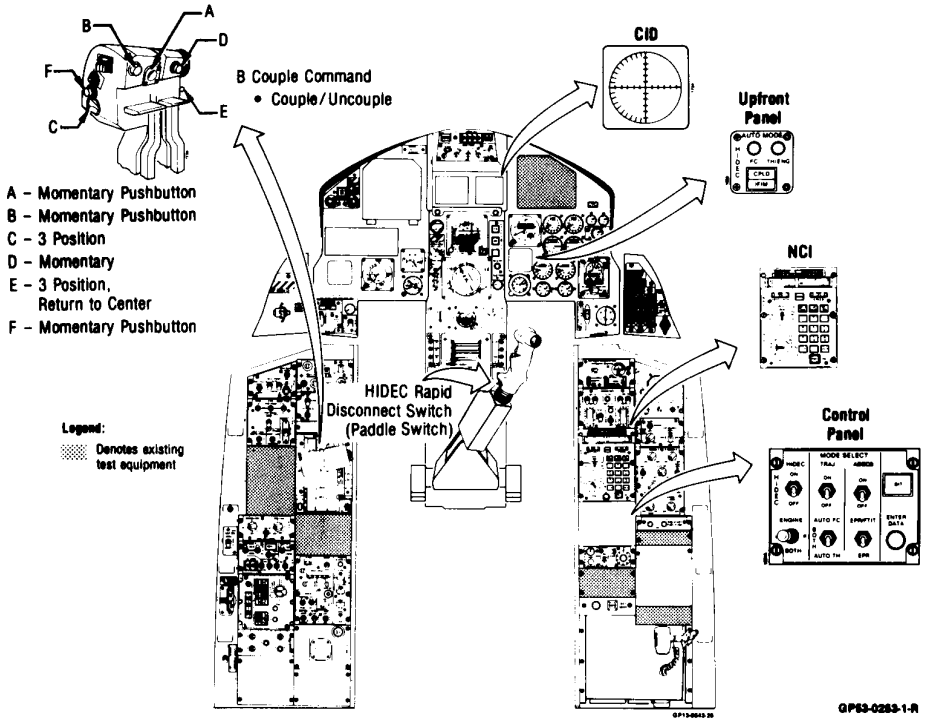

Fig. 9. HIDEC crew station orientation.

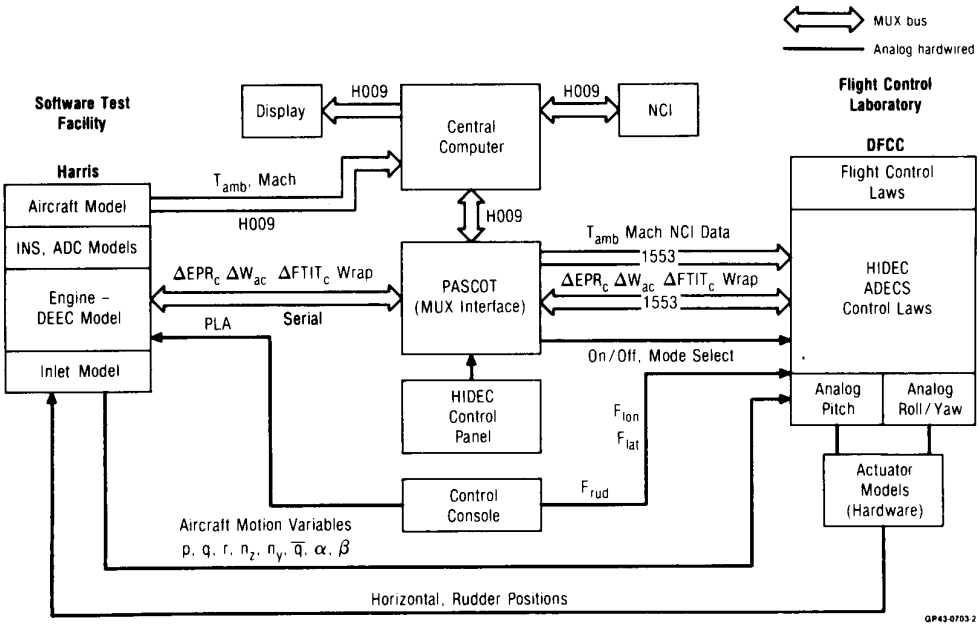

Fig. 10. HIDEC laboratory integration testing, ADECS mode.

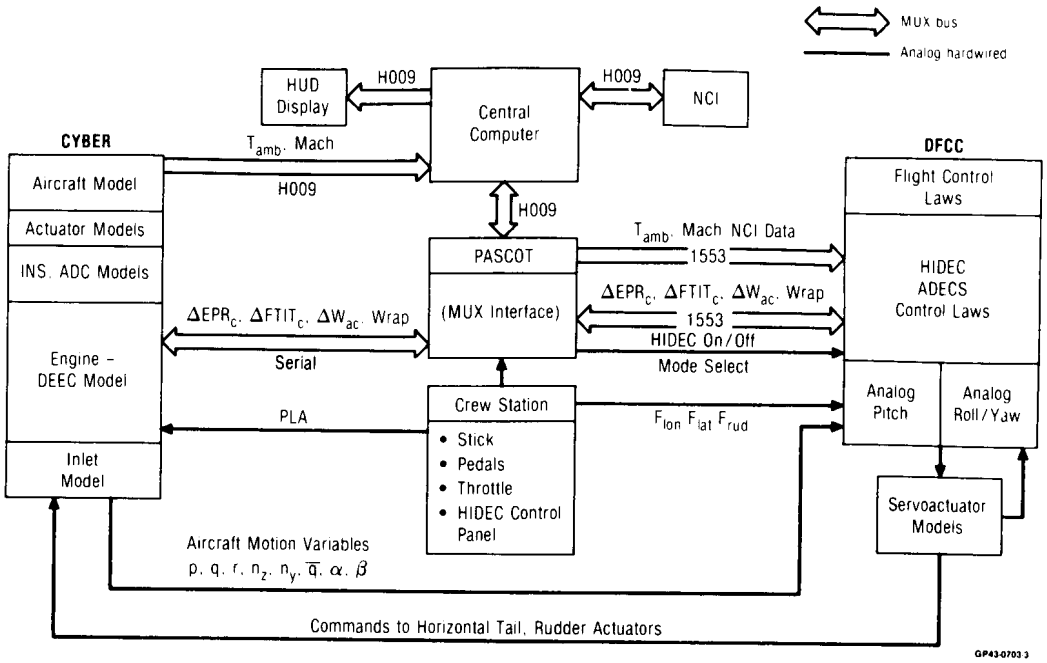

Fig. 11. HIDEC manned simulation testing, ADECS mode.

1. Report No.	2. Government Accession No.	3. Recipient's Catalog No.
NASA TM-86793		

4. Title and Subtitle	5. Report Date
Highly Integrated Digital Electronic Control — Digital Flight Control, Aircraft Model Identification, and Adaptive Engine Control	March 1987
	6. Performing Organization Code

7. Author(s)	8. Performing Organization Report No.
Jennifer L. Baer-Riedhart, NASA Ames-Dryden Flight Research Facility, and Robert J. Landy of McDonnell Aircraft Company, St. Louis, Missouri	H-1318
	10. Work Unit No. RTOP 533-02-21
9. Performing Organization Name and Address NASA Ames Research Center Dryden Flight Research Facility P.O. Box 273 Edwards, CA 93523-5000	11. Contract or Grant No.
	13. Type of Report and Period Covered Technical Memorandum
12. Sponsoring Agency Name and Address National Aeronautics and Space Administration Washington, DC 20546	14. Sponsoring Agency Code

15. Supplementary Notes

Prepared as AIAA Paper 85-1877 for presentation at the AIAA Guidance and Control Conference, Snowmass, Colorado, August 19-21, 1985.

16. Abstract

The highly integrated digital electronic control (HIDEC) program at NASA Ames Research Center, Dryden Flight Research Facility is a multiphase flight research program to quantify the benefits of promising integrated control systems. McDonnell Aircraft Company is the prime contractor, with United Technologies Pratt & Whitney Aircraft, and Lear Siegler Incorporated as major subcontractors.

The NASA F-15A testbed aircraft was modified for the HIDEC program by installing a digital electronic flight control system (DEFCS) and replacing the standard F100 (Arab 3) engines with F100 engine model derivative (EMD) engines equipped with digital electronic engine controls (DEEC), and integrating the DEEC's and DEFCS. The modified aircraft provides the capability for testing many integrated control modes involving the flight controls, engine controls, and inlet controls.

This paper focuses on the first two phases of the HIDEC program, which are the digital flight control system/aircraft model identification (DEFCS/AMI) phase and the adaptive engine control system (ADECS) phase.

17. Key Words (Suggested by Author(s))	18. Distribution Statement
Adaptive engine stall margin; advanced F100 engine; digital electronic engine control (DEEC); F-15 aircraft; flight test; flight-path management; increased thrust; improved operability; integrated control;	Unclassified — Unlimited Subject category 07

19. Security Classif. (of this report)	20. Security Classif. (of this page)	21. No. of Pages	22. Price*
Unclassified	Unclassified	14	A02

*For sale by the National Technical Information Service, Springfield, Virginia 22161.