

Procedure Integrated Development Environment (PRIDE)

S&K Aerospace

Technical Abstract

NASA captures and distributes operational knowledge in the form of procedures. These procedures are created and accessed by a range of people performing many different jobs. These people have different needs for procedure data and different ways of interacting with procedures. We propose an Procedure Integrated Development Environment which will present different editing modes and different views depending on the users and tasks, but will use a consistent data representation for all users. We propose to connect the editing environment to other tools and systems that are useful to procedure development, including recon databases and verification tools. We propose to build this environment on the basis of an existing prototype, PRIDE, which was developed for the Engineering Directorate of Johnson Space Center.

Company Contact

Arthur Molin
(281) 480-1453
amol@ska-corp.com

Efficient Techniques for Formal Verification of PowerPC 750 Executables

Aries Design Automation, LLC

Technical Abstract

We will develop an efficient tool for formal verification of PowerPC 750 executables. The PowerPC 750 architecture is used in the radiation-hardened RAD750 flight-control computers that are utilized in many space missions. The resulting tool will be capable of formally checking: 1) the equivalence of two instruction sequences; and 2) properties of a given instruction sequence. The tool will automatically introduce symbolic state for state variables that are not initialized and for external inputs. We bring a tremendous expertise in formal verification of complex microprocessors, formal definition of instruction semantics, and efficient translation of formulas from formal verification to Boolean Satisfiability (SAT). We will also produce formally verified definitions of the PowerPC 750 instructions used in the project, expressed in synthesizable Verilog; these definitions could be utilized for formal verification and testing of PowerPC 750 compatible processors, for FPGA-based emulation of PowerPC 750 executables, as well as in other formal verification tools to be implemented in the future.

Company Contact

Miroslav Velev
(773) 856-6633
miroslav.velev@aries-da.com